# AQR107-AQR109
# AQrate® Multi-Gigabit Ethernet PHY Transceiver

## General Description

The Aquantia® AQR107-AQR109 AQrate PHYs are low-power, full-reach, high-performance, multi-gigabit (10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX) Ethernet PHY transceivers. Aquantia AQrate PHYs are compliant with both the IEEE® 802.3an/bz standard and the NBASE-T™ Alliance PHY Specification to perform all of the physical layer functions required to implement 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX transmission over 100+ meters of twisted pair cabling. The AQrate PHY family integrates such features as Energy Efficient Ethernet (EEE), Precision Time Protocol (PTP)/1588v2, IEEE MAC Security (MACsec), supports all PoE standards up to 100W, and supports jumbo packets up to 16KB in all operating modes.

The AQR107-AQR109 are pin-compatible, multi-gigabit PHYs housed in compact 7 mm x 11 mm flip-chip BGA packages and operate over both the Extended (0°C to +108°C) and Industrial (-40°C to +108°C) temperature ranges. Unless otherwise noted, the datasheet describes 5-speed operation and functionality.

| Features | Benefits |
|---|---|
| • AQR107: 10GBASE-T/5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX<br>• AQR108: 5GBASE-T/2.5GBASE-T/1000BASE-T/100BASE-TX<br>• AQR109: 2.5GBASE-T/1000BASE-T/100BASE-TX | • Pin-compatible multi-gigabit PHYs (5-speed/4-speed/3-speed) enable design flexibility and reuse |
| • IEEE 802.3an/bz and NBASE-T featuring AQrate technology<br>o 10GBASE-T: 100 meters over Augmented Cat 6 (Cat 6A) and Cat 7, 55 meters over Cat 6, and best effort over Cat 5e<br>o 5GBASE-T, 2.5GBASE-T: over 100 meters of Cat 5e or better cabling | • Ability to support highest data rate possible with a given cable environment while reducing power and latency<br>• 5G and 2.5G operation over legacy infrastructure, while delivering backward compatibility with existing equipment |
| • 2.7W typical 10GBASE-T operating power per port<br>o 30 meters of Cat 6A UTP<br>• 2.3W typical 5GBASE-T operating power per port<br>• 1.9W typical 2.5GBASE-T operating power per port | • Enables efficient high-density design for high port-count and compact switches across a range of speed requirements |
| • Energy-Efficient Ethernet (EEE)<br>• MACsec (IEEE 802.1ae, MAC security standard)<br>o Full support for Advanced Encryption Standard (AES-256) and stand-alone operation<br>• PTP/1588v2<br>• Synchronous Ethernet (Sync-E), ITU-T standard in cooperation with IEEE | • EEE lowers overall power consumption and lowers equipment operating costs<br>• MACsec provides for secure, encrypted data communications across networks<br>• PTP/1588v2 provides for timing accuracy across the network<br>• Sync-E synchronizes clock signals on the PCB |
| • Integrated Wake-on-LAN (WoL) Support<br>o Compliant to Microsoft Network Device Class specification<br>• Energy Detect<br>o Places PHY in a low-power state when there is no active link partner | • Integrated packet filtering enables sub-1W support in 100BASE-TX mode<br>• Provides additional power savings when no active link partner is present |
| • Built-in Thermal Management<br>o On-chip thermal sensor with alarm and warning thresholds | • Enables deployment in thermally constrained environments |
| • 7 mm x 11 mm flip-chip 104-pin BGA package<br>o 0.8 mm ball pitch<br>o Low thermal resistance | • Low cost<br>• Flexible heat-sinking<br>• Compatible with volume PCB manufacturing |
| • IEEE ® 802.3-2012 compliant auto-negotiation | • Interoperable with existing Ethernet infrastructure |
| • External SPI FLASH interface with optional FLASH-less operation<br>o At-manufacture FLASH burn capability | • Reduces BOM cost as one or no FLASH devices required<br>• Enables firmware download/upgrade and FLASH image loading during manufacturing |

| Features | Benefits |
|---|---|
| • 50MHz Crystal or Differential Clock Operation<br>o Integrated ultra-low phase noise synthesizer<br>• 50MHz output clock signal | • Crystal operation allows for lower BOM cost<br>• Outputs primary and secondary 50MHz received reference for Sync-E |
| • Advanced Cable Diagnostics<br>o On-chip high-resolution cable analyzer | • Enables the deployment of meaningful cable analysis tools for debugging installation problems |
| • High-Performance full KR (with autonegotiation)/XFI/USXGMII/ 2500BASE-X/SGMII I/F w/ AC-JTAG<br>o Capable of rate adapting all rates into KR/XFI via PAUSE and 100M/1G into 2500BASE-X | • Ensures trouble-free operation over a range of interconnect scenarios<br>• Comprehensive interface support<br>o Supports legacy and next generation MACs/switches/ processors |
| • Advance Loopback and Diagnostic Capability<br>o Flexible on-chip BERT<br>o Full 1 second packet counters and CRC-32 checkers | • Enables extensive system test and debug with remote loopback control |
| • Integrated MDI Filter and Advanced RFI Cancellation<br>o Eliminates external filter components | • Robust Radio Frequency Interference (RFI) performance<br>o Resilient operation when exposed to RFI |

## Detailed Description

A block diagram of the AQR107-AQR109 is shown in Figure 1. Each port utilizes a common analog front-end for all 5 modes of operation, and a common system interface (configurable as KR or XFI in 10G, 2500BASE-X in 2.5G, and SGMII in 1G/100M, or all rates via USXGMII/KR). In the transmit direction in 10G, and AQrate modes, data from the system interface is equalized and received.

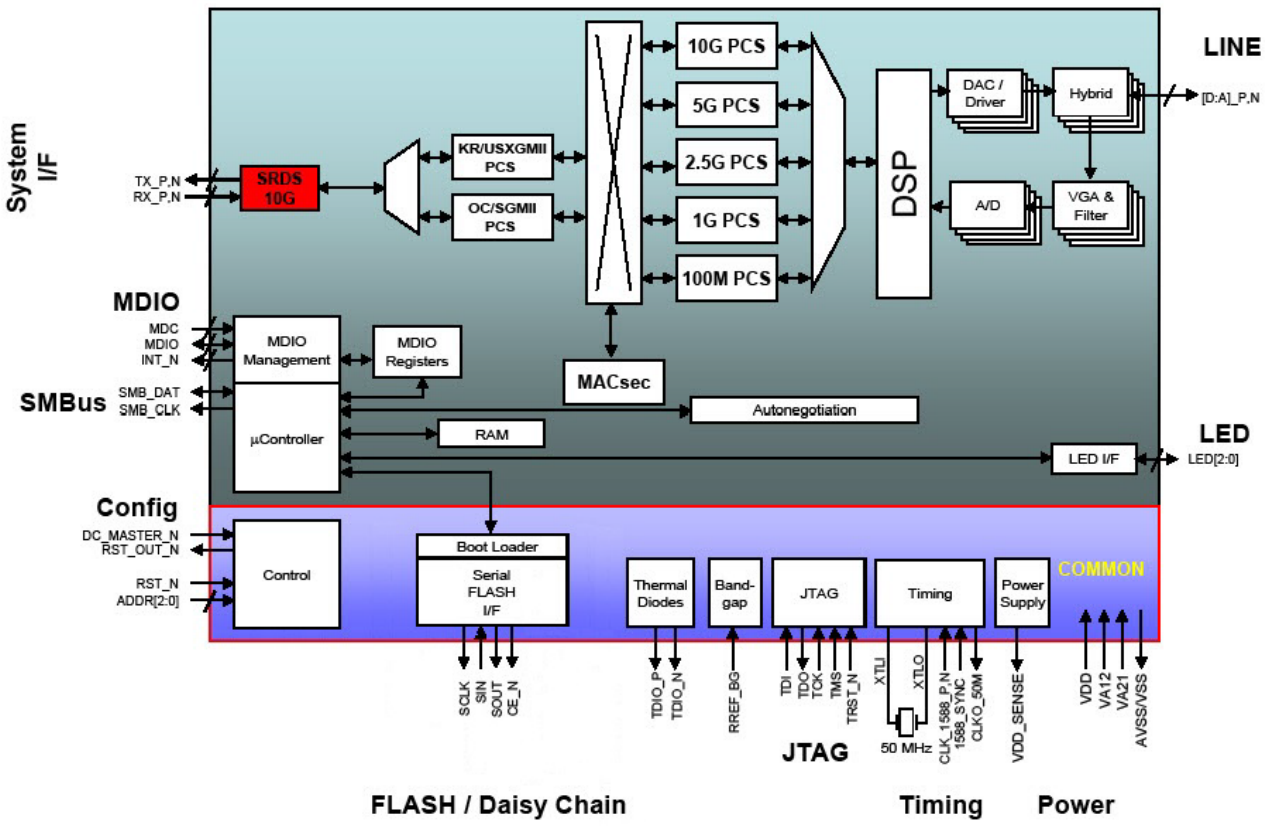


*Figure 1* **AQR107-AQR109 Block Diagram**

This data is then mapped into a virtual internal XGMII interface where blocks of two XGMII frames (32 bits of data + 4 bits of control) are encoded into a single 65B block, using the 64B/65B encoding scheme specified in Clause 55. In 10G mode, fifty of these 65B blocks are aggregated together, along with a prepended auxiliary bit, and an appended CRC-8 to form the 3259-bit 10GBASE-T transmission frame payload.

This payload is encoded using a combination of LDPC encoding and coset partitioning, with the LDPC encoding adding an additional 325 systematic check bits to produce a 3584-bit 10GBASE-T transmission frame. The coset partitioning effectively divides the frame up into 512 7-bit symbols, where the upper 3 bits are uncoded and describe the coset, while the lower 4 bits are coded and identify an element within the coset.

These 8 cosets are then mapped onto a 128-DSQ constellation (a 16 x 16 checkerboard pattern) which is physically encoded as two back-to-back PAM-16 symbols. These symbols are then THP precoded, filtered, and sent out over the four twisted pairs in the cable. AQrate 5G transmission is done in a similar fashion, but uses a fully LDPC encoded 320ns PAM-16 frame containing twenty-five 65B blocks. AQrate 2.5G transmission is also similar, but uses a 640ns frame containing twenty-five 65B blocks.

In the receive direction in 10G, 5G, and 2.5G modes, PAM-16 coded symbols enter the AQR107-AQR109 from the line interface and pass through the hybrid, which provides transmit / receive isolation. These symbols are then filtered and amplified prior to being sampled by four high-speed, high-precision A/D converters. The outputs of these A/D converters are then passed through an extensive set of adaptive equalizers which provide both cross-talk and echo cancellation. After timing is recovered, the data from the four channels is aligned and merged together to form the original, but noisy transmission frames.

In all three modes, the data is decoded using an LDPC decoder. However, in 10G mode the data is further sliced using knowledge of the coset partitioning and 128-DSQ mapping to produce the original 10GBASE-T transmission frame payload. The CRC-8 over this payload is then checked to ensure integrity of the uncoded bits. Finally, in all schemes, the auxiliary bit is stripped, the 65B blocks remapped into XGMII blocks, and the received Ethernet data transmitted out the MAC interface.

When operating in 1G or 100M modes, receive data from the analog front-end is routed to either the 1G or 100M PCS where timing is recovered and equalization performed. In 1G mode, Viterbi decoding is also done. From here, the data passes across a virtual GMII interface to the system interface which is either SGMII, or USXGMII mode on logical Lane 0.

In the transmit direction, 1G or 100M data is received on either the SGMII, or USXGMII interface, passed through the 1G or 100M PCS and then transmitted by the common analog front-end. Figure 2 shows a typical system-level block diagram of a 10GBASE-T channel built using the AQR107-AQR109.

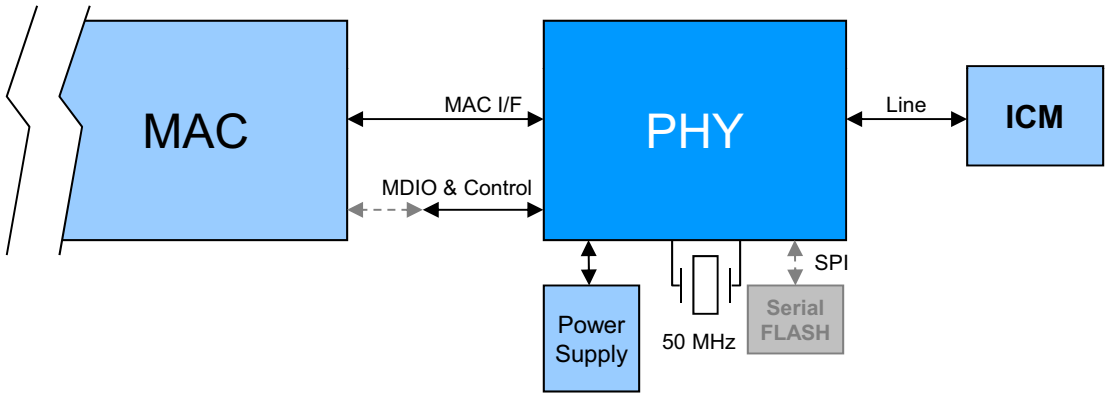


*Figure 2* **AQR107-AQR109 System Block Interconnect**

On the line side of the AQR107-AQR109, a robust interface providing good common-mode rejection and electrical protection against cable discharge is implemented. On the MAC side, the AQR107-AQR109 provides a robust SerDes interface with configurable pre-emphasis and receive equalization. For test coverage, this interface also incorporates AC JTAG.

Control over the chip is done via an external C-language application program interface (API) that provides an easy-to-use abstraction of the AQR107-AQR109, and via an MDIO interface provides the standard Clause 45 register set for control of 10GBASE-T devices.

On-chip, the AQR107-AQR109 contains a 32-bit microcontroller which manages the state machines and operation of the various elements within the chip. Consequently, there is a great deal of flexibility afforded to the end user because of the presence of this microcontroller, and as such the AQR107-AQR109 offers a high degree of control and flexibility. The image for the microcontroller is stored either in an optional external SPI FLASH, or loaded at boot time via the MDIO interface (MDIO boot-load).

This interface also provides the user the capability of directly programming the FLASH during manufacturing. In addition to the Ethernet interfaces, the AQR107-AQR109 provides three 20mA LED outputs for the port that are software configurable to respond to a variety of conditions such as link activity and connection status. Clocking for AQR107-AQR109 is provided from a 50MHz external crystal or differential clock.

To better assist the system designer in deploying the AQR107-AQR109, a reference design (with part numbers, schematics, and layout) is provided that is optimized for performance, efficiency, and cost. Power for the AQR107-AQR109 is provided from three supply voltages, and supports I/O voltage levels of 1.8V and 3.3V.

## Package Information

The AQR107-AQR109 is packaged in a 0.8 mm pitch, 7 mm x 11 mm over-molded flip-chip BGA (8 rows x 13 rows). The package is marked as shown in Figure 3, and is described in Table 1 on page 5.

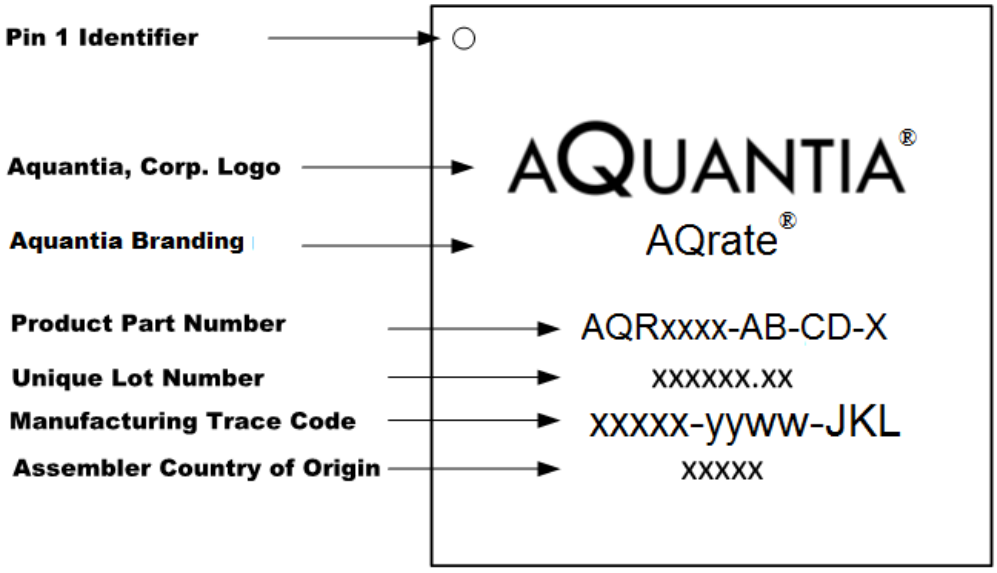


*Figure 3* **Part Marking**

| Part of Code | Description | Available Options |
|---|---|---|
| AQRnnnn | Product Name | Refer to master part number specification for specifics. |
| A | Base Layer Rev Control | A: First all-layer mask<br>B: Second all-layer mask |
| B | Metal Layer Rev Control | 0: First or original rev of silicon<br>1: First metal-only tape-out<br>2: ..... |
| C | Temperature Grade | E: Extended (0°C – 108°C)<br>I: Industrial (-40°C – 108°C) |
| D | Restriction of Hazardous Substances (RoHS) Type | G: Green (6/6); lead-free bump and lead-free BGA balls |
| X | Customer-Specific Indicator | Field is reserved as an "add mark" field for customer-specific versions of Aquantia products |

**Table 1: Part Marking Descriptions**

## Release Notes

The *Aquantia* AQR107-AQR109 *Release Notes* must be consulted for a full list of known issues and errata associated with AQR107-AQR109.

## Ordering Information

| Part Number | Description | Ordering Part Number |
|---|---|---|
| AQR107 | Silicon Rev. B0, 5-Speed Extended Temp Grade, RoHS 6/6 | AQR107-B0-EG-Y |
| AQR107 | Silicon Rev. B0, 5-Speed Industrial Temp Grade, RoHS 6/6 | AQR107-B0-IG-Y |
| AQR108 | Silicon Rev. B0, 4-Speed Extended Temp Grade, RoHS 6/6 | AQR108-B0-EG-Y |
| AQR108 | Silicon Rev. B0, 4-Speed Industrial Temp Grade, RoHS 6/6 | AQR108-B0-IG-Y |
| AQR109 | Silicon Rev. B0, 3-Speed Extended Temp Grade, RoHS 6/6 | AQR109-B0-EG-Y |
| AQR109 | Silicon Rev. B0, 3-Speed Industrial Temp Grade, RoHS 6/6 | AQR109-B0-IG-Y |

## Contact Information

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# Table of Contents

Section Page

# Table of Contents

# Table of Contents

# Table of Contents

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# Table of Contents

Section Page

# List of Figures

# List of Figures

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

Table Page

# List of Tables

# List of Tables

# List of Tables

Table Page

# List of Tables

# List of Tables

Table Page

# List of Tables

AQUANTIA®

# List of Tables

Table Page

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

# List of Tables

Table Page

# List of Tables

# List of Tables

# List of Tables

Table Page

# Overview 1

## 1.1 Introduction

The AQR107-AQR109 is a single-port, multi-gigabit CMOS PHY designed to be a low-power, stand-alone solution for all NIC, switch, and LAN-on-Motherboard (LoM) applications that require multi-gigabit capability, and supports the following network rates:

- 10GBASE-T
- 5GBASE-T
- 2.5GBASE-T
- 1000BASE-T
- 100BASE-TX

This chapter provides an overview of the AQR107-AQR109 and its operating modes.

## 1.2 General Deployment

This section briefly touches on the hardware implementation. For more detailed hardware design information, please see the *Aquantia Hardware Design Guide* (see “Hardware Design Guide”, Aquantia Corporation" on page 591).

### 1.2.1 Mechanical

The AQR107-AQR109 is packaged in a 7 mm x 11 mm flip-chip 104-pin BGA (8 rows x 13 rows). The die is rated to operate up to 108°C junction temperature, so engineering an appropriate thermal solution for the target system is designed to be a straight-forward task.

### 1.2.2 Power Supplies

The AQR107-AQR109 utilizes four power supplies:

- A 0.85V digital supply (VDD)
- Two analog supplies:1.2V and 2.1V(VA12 and VA21, respectively)
- A configurable I/O supply (VDD_IO)

All supplies should come up within 100ms from the first rail rising to the last rail reaching its 70% voltage level. The proper power-up sequence requires the VDD and 1.2V rails reach nominal voltage levels in any order first, followed by the other power rails in any order (this same order must be followed for the power-down sequence).

For the I/O supply, the AQR107-AQR109 offers a configurable VDD_IO that supports both 1.8V and 3.3V, and this will set the logic thresholds for the I/O at 70%/30% of its voltage.

**Note:** AVSS, VSS, and VSS_SRDS must be tied to the same ground plane.

### 1.2.3 Reset

The AQR107-AQR109 supports on-chip power-on reset generation and it is also capable of supplying this reset to the rest of the system via a RST_OUT_N pin.

### 1.2.4 Clocks

The AQR107-AQR109 uses either a 50MHz crystal or a 50MHz LVDS differential clock to synthesize all of the required clocks. For Synchronous Ethernet (Sync-E) applications, the AQR107-AQR109 is capable of outputting to the system a 50MHz clock phase-locked to the line clock.

### 1.2.5 FLASH

The AQR107-AQR109 is capable of operating with a 512KByte (4Mbit) or larger SPI serial FLASH for autonomous operation, or of being boot-loaded via the MDIO interface. In both cases, the image stored in FLASH and the MDIO boot-load image are identical. If autonomous operation is not a requirement, and the target system is capable of providing the boot-load image, the FLASH can be eliminated.

The FLASH I/O operating voltage level must be the same as the PHY's VDD_IO voltage level. If boot-loading is desired, it is possible to gang-load multiple parts via a broadcast MDIO address in the AQR107-AQR109.

### 1.2.6 Power-On Default Values

The AQR107-AQR109 has a fixed set of hardware default values that exist in the chip for all configurable registers. However, the firmware is capable of storing in its boot image (or in a separate image to keep the base firmware constant across multiple platforms) any change to these defaults effectively allows the user to configure the chip to come out of reset in the desired operating state.

### 1.2.7 SerDes and MDI Configuration

In order to offer routing flexibility on the SerDes interface, the AQR107-AQR109 is capable of performing polarity inversions[†].

[†] Note that polarity inversion is also referred to as "Lane Invert" in the register map.

On the line side, in addition to supporting MDI/MDI-X and automatic polarity correction, the AQR107-AQR109 supports lane swapping of the ABCD pairs to enable easy board routing with different magnetics pin-outs.

## 1.3 SerDes

The AQR107-AQR109 is designed to be used in conjunction with a five-speed MAC chip. Table 1.1 and Table 1.2 detail the idle and operating modes of the AQR107-AQR109 interface:

| System I/F Idle Mode | Notes |
|---|---|
| Off | SerDes turns on at selected operating mode for rate |
| XFI + USXGMII | |
| KR + USXGMII | |

*Table 1.1* **System I/F Idle Options**

The AQR107-AQR109 PHY device family supports the following SerDes modes.

| Operating Modes | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Rates** | **SGMII** | **1000BASE-X** | **KX** | **2500BASE-X** | **USXGMII** | **XFI** | **KR** |
| 100M | ✓ | | | ✓ | ✓ | ✓ | ✓ |
| 1G | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| 2.5G | | | | ✓ | ✓ | ✓ | ✓ |
| 5G | | | | | ✓ | ✓ | ✓ |
| 10G | | | | | ✓ | ✓ | ✓ |

*Table 1.2* **System I/F Operating Modes**

**Note:** In Table 1.2, the green check marks indicate native rate support and the orange check marks indicate rate-adaptation via PAUSE control.

## 1.4 Power-On

The AQR107-AQR109 is designed to perform the following operations at boot:

*1)* Power-up calibration of internal VCOs and variable power supplies (if variable supply operation is enabled)

*2)* Provision stored default values†

3) Calibration of the analog front-end

4) Autonegotiation

5) Perform training (as required)

6) Verify error-free operation

7) Enter steady state

## 1.5 Cable Diagnostics

The AQR107-AQR109 implements a powerful cable diagnostic algorithm to accurately measure all of the TDR and TDT† sequences within the group of four channels. The algorithm used transmits a pseudo-noise sequence with an amplitude of less than 300 mV for a brief period of time, and from this converges the 10GBASE-T equalizers on all of the other channels. From the results of this measurement, the length of each pair, the top impairment along the pair, and the impedance of the cable are flagged. These measurements are reported using cable propagation characteristics of 4.83ns/m and are presented in the Global MMD register map (for details, see “References” on page 591).

## 1.6 Debug and Diagnostics Tools

The AQR107-AQR109 supports a full suite of network and system loopbacks at all supported rates. The loopbacks are shown in Figure 1.1. In addition to the loopbacks, the AQR107-AQR109 supports CRC-32 packet checking on both the receive and transmit traffic at all supported rates, and maintains 1-second interval packet counters for both errored and good packets.

Finally, the AQR107-AQR109 is able to generate all of the IEEE test mode patterns, as well as CRPAT generation and checking in both line and system directions. It also supports (via the API) the ability to generate an eye diagram for each of the receive lanes.

On the KR interface, the AQR107-AQR109 supports $x^9$, $x^{31}$, square wave, and pseudo-noise generation and checking, as well as CRPAT generation and checking.

† The AQR107-AQR109 is capable of storing in its firmware image a list of registers whose default values should be overwritten with a user-specified value on power-up. This is done using the web-based Aquantia Firmware Provisioning Tool, and allows the PHY to be personalized for certain modes of operation.

† The cross-channel impulse responses.

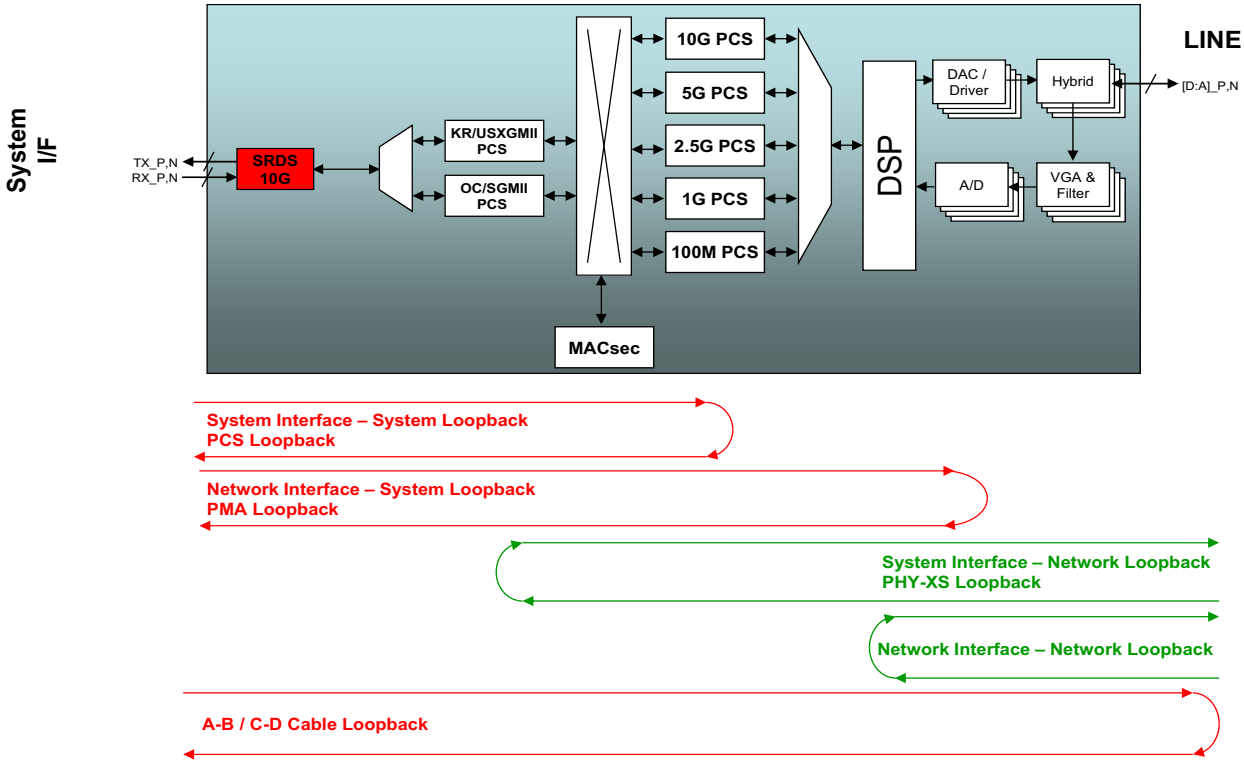


*Figure 1.1* **Loopbacks**

## 1.7 API and Programming Tools

Associated with the AQR107-AQR109 are the following software tools:

1) A set of ANSI C register structures for each MMD that provide bit level and word level access to all of the AQR107-AQR109 registers. Documentation for these structures are found in the API document (for details, see “References” on page 591).

2) An ANSI C API that provides a set of structures and associated Set / Get functions to implement all normal PHY operations. This API is written with register name abstraction so the registers are visible, and it is documented using Doxygen, which allows users to view the code and click on a variable to get the datasheet definition.

   This API also contains functions to burn new FLASH images, as well as perform MDIO boot-load operations, etc. Documentation for this is found in the API document (for details, see “References” on page 591).

## 1.8 MACsec

The AQR107-AQR109 supports integrated MACsec at all rates and supports the following modes of operation:

1) **Autonomous Operation**: In this mode, the AQR107-AQR109 does all of the gap insertion, etc. required to add the MACsec headers and integrity check values (ICVs). It does this via two integrated MACs and 64KB of buffering in each direction. These MACs monitor the buffer fill-depths, and generates port-based PAUSE frames in either direction as required. It also responds to port-based PAUSE frames. 802.1Qbb class-based PAUSE frames are passed through.

2) **Cut-through Operation**: In this mode, the AQR107-AQR109 expects to receive packets from the system pre-gapped, and all the AQR107-AQR109 does is insert the MACsec headers and ICVs.

3) **Bypass Operation:** In this mode, the MACsec block is completely bypassed, in scenarios where MACsec in the PHY is not necessary.

### 1.8.1 General Features

The MACsec supports the following general features:

1) AES-256, AES-128, and clear operation with simultaneous mixed usage, where the encryption and decryption are decided on a per-packet basis based on an access control list (ACL) that looks either at the MACsec header or fields in the packet header (explicit or implicit secure channel identification).

2) 16 secure channels (SCs), with two security associations (SAs) per SC with automatic roll-over between SAs on a programmable packet number (PN) value.

3) Full support of the 802.1AE MIB (for details, see “Media Access Control (MAC) Security”, IEEE STD-802.AE-2006, IEEE Standards Office, The Institute of Electrical and Electronics Engineers, Inc., 3 Park Avenue, New York, NY 10016-5997, USA, April 17, 2003).

4) Per packet Galois counter mode (GCM) authentication on the ICV (16 or 32 byte).

5) Strict and out-of-order replay checking with a per SC programmable 32-bit (i.e from 0 to $2^{31}$-1 packets) replay window for out-of-order mode.

6) A programmable confidentiality offset per SA of between 0 and 127 bytes offset.

7) A MIB containing the following additional statistics counters:

| Per SA | Name | Description |
|---|---|---|
| | Ingress Control Packets | The number of ingress control packets received |
| **X** | Ingress Untagged Hit Packets | The number of ingress untagged packets received that passed the implicit SCI lookup |
| | Ingress Untagged Miss Packets | The number of ingress untagged packets received that had no implicit SCI lookup |
| **X** | Ingress Hit Packets Dropped | The number of ingress packets that passed the SCI lookup, but were tagged for Drop |
| | Ingress Tagged Packets | The number of ingress packets with a MACsec header |
| | Ingress Tagged Packets Bad Tag | The number of ingress packets with an invalid SecTag or packet number (PN). |
| | Ingress Tagged Packets SCI Miss | The number of ingress tagged packets with a missing SCI or an SCI that was not in the table. |
| **X** | Ingress Tagged Packets Non-Operational SA | The number of ingress packets with an identified, but non-operational SA. |
| **X** | Ingress Packets Authentication Fail | The number of ingress packets that fail authentication |
| **X** | Ingress Packets Replay Fail | The number of ingress packets that fail the replay check |
| **X** | Ingress Packets Late | The number of ingress packets that fail the replay check because they are late |
| **X** | Ingress Packets OK | The number of ingress packets that pass all checks |
| | Ingress Reserved Counter 0 | |

*Table 1.3* **Additional Ingress MACsec Statistics**

| Per SA | Name | Description |
|---|---|---|
| | Ingress Reserved Counter 1 | |
| | Ingress Reserved Counter 2 | |
| | Ingress Reserved Counter 3 | |

*Table 1.3* **Additional Ingress MACsec Statistics** (continued)

| Per SA | Name | Description |
|---|---|---|
| | Egress Control Packets | The number of egress control packets transmitted |
| | Egress Packets Unknown SA | The number of egress packets transmitted with an unknown SA (Table Miss and Untagged) |
| | Egress Untagged Packets | The number of egress packets transmitted without a MACsec header |
| **X** | Egress Protected Packets | The number of egress packets transmitted with a valid ICV (authenticated + encrypted) |

*Table 1.4* **Additional Egress MACsec Statistics**

### 1.8.2 Ingress Lookup

On ingress, the MACsec block can:

*1)* Remove the MACsec header.

*2)* Strip zero-padded bytes for runt packets.

*3)* Corrupt the FCS for any failed packets.

*4)* Run a consistency check against another ACL.

*5)* Count control packets.

*6)* Enforce maximum MTU sizes via either truncation or FCS corruption.

*7)* Generate an interrupt on security failure.

8) Lookup the implicit SCI based on the following fields:

   a) MAC DA - 48 bits.

   b) MAC SA - 48 bits.

   c) Payload Ether-Type - 16 bits.

   d) QTAG_VLD and STAG_VLD (Ingress Consistency Check only).

   e) TCI / AN - 8 bits (Note TCI needs preprocessing as per Clause 9.1.2).

   f) SCI - 64 bits.

   g) VLAN - 12 bits (Ingress Consistency Check only).

   h) Any four programmable bytes within the first 64 bytes of the packet.

   i) Origin (loopback versus front panel) - ingress table only.

   j) Valid bit.

9) Lookup the implicit SCI based on the following fields:

   The MACsec block for the AQR107-AQR109 supports the ability to calculate the EtherType, VLAN, and User-Priority of a packet using a 32-bit mapping table that is provided with each entry in the SCI lookup.

   There is one mapping table per port and the mapping table contains the following fields:

| Bit | Name | Function |
|---|---|---|
| 31 | PARSE_QTAG | Enables parsing 802.1Q VLAN tags |
| 30 | PARSE_STAG | Enables parsing 802.1Q MST tags |
| 29 | PARSE_QINQ | Enables Q-in-Q parsing |
| 28 | QTAG_UP_EN | Enables the use of the 802.1Q priority |
| 27 | STAG_UP_EN | Enables the use of the 802.1S priority |
| 26:24 | DEF_UP | Represents default user-priority |
| 23:0 | MAP_TBL | Represents priority mapping for 802.1Q priority tags |

*Table 1.5* **"Per SCI" 32-Bit Mapping**

EtherType, VLAN, and User-Priority of a packet are determined as follows (using this mapping table):

*a)* EtherType and VLAN resolution is determined as shown in Figure 1.2 (802.1S and 802.1Q EtherTypes are provisionable per port.

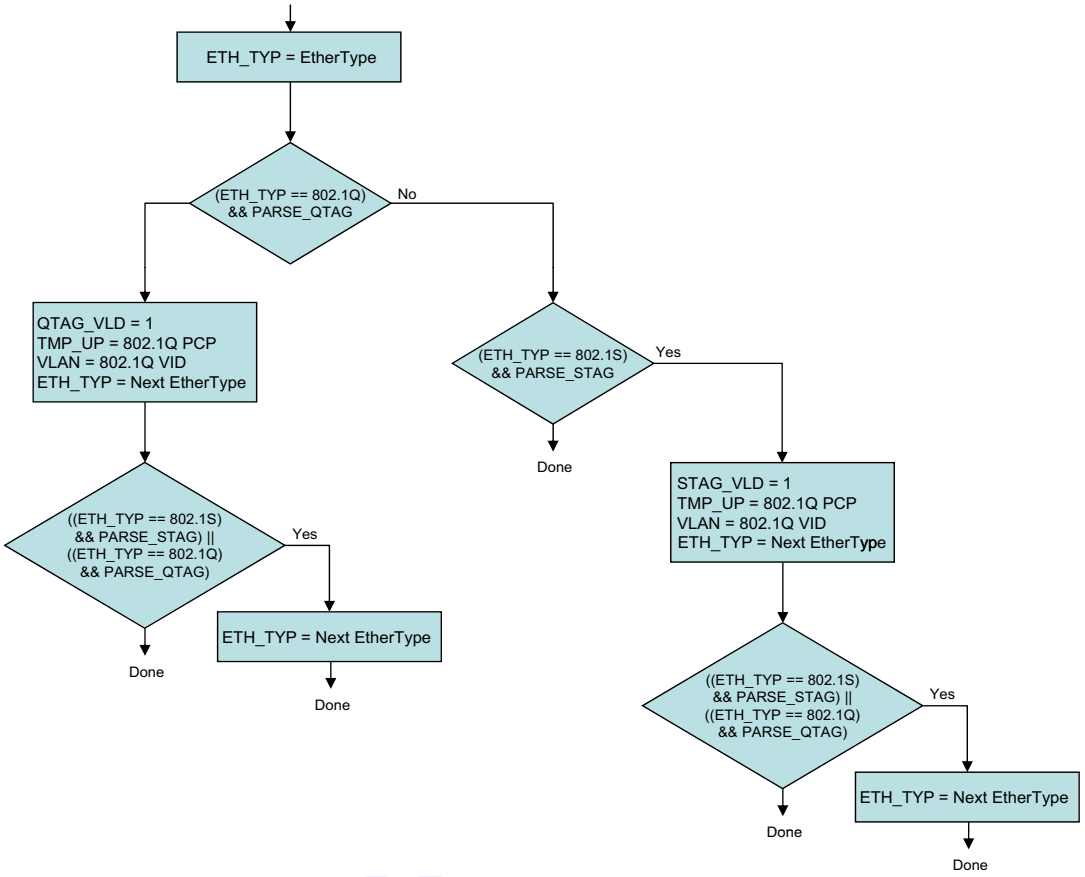


*Figure 1.2* **EtherType and VLAN Parsing Algorithm**

*b)* User priority is resolved as shown in Figure 1.3:

*10)* Support a provisioned definition of the 802.1Q and 802.1S EtherType tags.

*11)* Support the following actions from the SCI lookup:

*a)* Decrypt/Authenticate (provisioned per SA).

*b)* Drop.

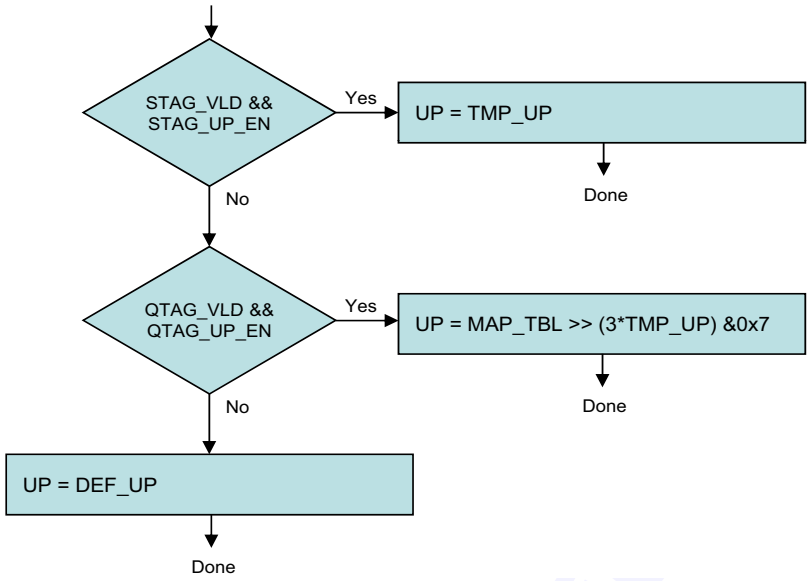


*Figure 1.3* **User priority resolution**

*c)* Bypass.

*d)* Re-direct (capture to debug).

*12)* Support globally changing the action for the lookup on a table basis (for allowing rapid debug).

### 1.8.3 MACsec Ingress Post-Processing

After decryption during post-processing, the MACsec block can:

*1)* Remove or leave the MACsec header.

*2)* Over-write the PN field of the MACsec header with provisionable data when operating in MACsec header non-removal mode.

*3)* Strip zero-padding bytes from the packet according to the MACsec header short-length (SL) field.

*4)* Grow short packets that are not SL stripped back to 64-bytes (for example, the MACsec packet is ≥ 64 bytes, but after removal of the MACsec, the packet is sub-64 bytes).

5) Support the corruption of the FCS on packets which fail any enabled security check in both the ingress and egress directions.

6) Support a 32 entry per port consistency check after decryption based on:

   a) SAI_HIT

   b) SAI[3:0]

   c) VLAN[11:0]

   d) VLAN_VLD

   e) ETYPE_VLD (EtherType > Programmable max length)

   f) Payload EtherType[15:0]

   g) Each of these fields shall be maskable and have a single action bit indicating whether to drop the packet or not.

   h) The port shall also support a 33rd entry indicating what to do with a miss.

7) Generate an interrupt on security failure.

### 1.8.4 Egress Processing

On egress, the MACsec block can:

1) Support the same lookup and mapping mechanism as is used in the ingress direction.

2) Support the ability to perform lookup with and without the presence of a MACsec header.

3) Zero pad short packets and mark the SL field in the MACsec header accordingly.

4) Fill in the remainder of the MACsec header, given provided TCI and SL fields. This means that the MACsec EtherType (88_E5), AN, PN, and optional SCI are filled in by the PHY.

5) Support the following actions from the SCI lookup:

   a) Encrypt/Authenticate (provisioned per SA).

   b) Drop.

   c) Bypass.

   d) Re-direct (loopback or capture to debug).

6) Count control packets.

7) Enforce maximum MTU sizes via either truncation or FCS corruption.

8) Support globally changing the action for the lookup on a table basis (for allowing rapid debug).

9) Generate an interrupt on security failure.

### 1.8.5 MACs

The MACs in the MACsec block can:

1) Support ingress and egress MIBs with per-EtherType 40-bit counters and RMONs (packet drop and packet pass-through).

2) In store-and-forward mode shall support port-based PAUSE flow-control in both directions, with programmable thresholds and hysteresis.

3) Ignore 802.1Qbb class-based PAUSE frames and pass them through the PHY.

4) Support programmable ingress and egress inter-packet gap (IPG) of between 4 and 63 bytes†.

5) Support processor access to the MAC buffers for debug.

6) Support the ability to recognize control packets via the following criteria:

   a) MAC_DA[47:4] = 01_80_C2_00_00_0.

   b) MAC_DA[47:4] = 01_00_0C_CC_CC_CC.

† With each packet having a fixed 7-byte preamble and 1-byte start-of frame delimiter (SFD).

*c)* 8 per port programmable MAC_DA addresses.

*d)* 8 per port programmable EtherType matches.

*e)* 1 per port programmable MAC_DA with Don't Care mask.

*f)* 2 sets of per port programmable MAC_DA and EtherType combinations.

These shall be provisionable on a port by port basis.

*7)* Support sending and receiving up to 512 byte packets in both the ingress and egress directions.

Both the ingress and egress ports shall each support a programmable MAC address, and the ability to disable operation of these ports.

*8)* Support a non-destructive L2 system loopback, with a programmable MAC address and an enable. This loopback FIFO shall be 512 bytes in size and shall support head and tail drop (provisionable). This FIFO shall be capable of being stopped at any time (on a packet-by-packet granularity) and the packet(s) within read out.

The depth of this FIFO shall be programmable. Packets larger than a programmable size can be dropped or truncated (programmable). Packets which are dropped due to overflow must be counted on a per SA basis using an 8-bit counter (saturating, clear-on-read).

These looped-back packets must be accounted for in a similar set of counters to the ingress MAC, as they are not accounted for there (for example, the loopback after ingress MAC).

*9)* Enforcing a per priority, programmable maximum MTU size with an option for either truncation or FCS corruption.

*10)* Support the following statistics on ingress and egress (see Table 1.6):

*11)* Count MAC control packets that are either secured, unsecured, or both.

| Egress | Ingress | Per Priority | Name | Description |
|---|---|---|---|---|
| X | X | | Total Packets | The total number of packets (good + bad) |
| X | X | X | Total Packets (per priority) | The total number of packets (good + bad) (per priority) |
| X | X | | Dropped Packets | Packets dropped for any reason |
| X | X | X | Dropped Packets (per priority) | Packets dropped for any reason (per priority) |
| X | X | | Bytes | Total frame octets |
| X | X | X | Bytes (per priority) | Total frame octets (per priority) |
| X | X | | Broadcast Packets | Total broadcast packets with a good FCS |
| X | X | | Multicast Packets | Total multicast packets with a good FCS |
| X | X | | Fragments | Frames < 64 bytes with a bad FCS |
| X | X | | Jabbers | Frames > $MTU_{MAX}$ with a bad FCS |
| | X | | CRC Align Errors | Frames with a bad FCS that are neither fragments nor jabbers in-the-clear |
| X | | | Bad Packets | Frames with a bad FCS |
| X | | | Good Packets | Frames with a good FCS |
| | X | | Undersize Packets | Frames with a good FCS less than 64 bytes |
| X | X | | 64 Byte Packets | The total number of packets (good + bad) of 64 byte length |
| X | X | | 65 To 127 Byte Packets | The total number of packets (good + bad) between 65 and 127 byte length |
| X | X | | 128 To 255 Byte Packets | The total number of packets (good + bad) between 128 and 255 byte length |
| X | X | | 256 To 511 Byte Packets | The total number of packets (good + bad) between 256 and 511 byte length |

*Table 1.6* **MAC Statistics**

| Egress | Ingress | Per Priority | Name | Description |
|---|---|---|---|---|
| X | X | | 512 To 1023 Byte Packets | The total number of packets (good + bad) between 512 and 1023 byte length |
| X | X | | 1024 To 1518 Byte Packets | The total number of packets (good + bad) between 1024 and 1518 byte length |
| X | X | | 1519 To 1522 Byte Packets | The total number of packets (good + bad) between 1519 and 1522 byte length |
| X | X | | 1523 To 1548 Byte Packets | The total number of packets (good + bad) between 1523 and 1548 byte length |
| X | X | | 1549 To 2000 Byte Packets | The total number of packets (good + bad) between 1549 and 2000 byte length |
| X | X | | 2001 To 2500 Byte Packets | The total number of packets (good + bad) between 2001 and 2500 byte length |
| X | X | | 2501 To MTU Byte Packets | The total number of packets (good + bad) between 2501 and MTU byte length in-the-clear |
| X | X | | 1549 To MTU Byte Packets | The total number of packets (good + bad) between 1549 and MTU byte length in-the-clear |
| X | X | X | Oversize Packets (per priority) | The total number of packets of length greater than MTU bytes and a good FCS in-the-clear |
| X | X | | MAC Control Packets | MAC Control Frames with EtherType 88_08 in-the-clear or secured (option for both) |
| | X | | Errored Packets | Packets with Code or Symbol Errors |

*Table 1.6* **MAC Statistics** (continued)

## 1.9 Energy Efficient Ethernet

The AQR107-AQR109 provides support for EEE on both the system interfaces and line interfaces: supported system interfaces include SGMII and XFI/KR/USX; while on the line side, EEE is supported for 10GBASE-T, 5GBASE-T, 2.5GBASE-T, and 1000BASE-T. It is also capable of running in both a normal operating mode, where the system controls entering and exiting from the EEE state, and also autonomous operations on the line, where the PHY controls the entering and exiting EEE operation via a provisionable “no-traffic” timer.

If no traffic is seen within a certain period of time, the line side of the PHY goes to LPI (sleep) mode if it is connected to any of the supported rates. This operating mode requires that the MACsec buffers and MACs be in operation. MACsec buffers are required in internal mode to buffer the packet while the line is being restored to operational mode. The system side operates in normal non-EEE mode while the line side operates in EEE mode.

## 1.10 Precision Time Protocol (PTP)

The AQR107-AQR109 provides support for PTP and related protocols. Specifically it supports the following protocols (running both over MACsec or in the clear):

*1)* 1588 Version 1 (1-step and 2-step).

*2)* 1588 Version 2 (1-step and 2-step).

*3)* NTP Version 3.

*4)* NTP Version 4.

*5)* SNTP Version 4.

To support these protocols, the AQR107-AQR109 has the following counters:

*1)* A 48-bit seconds counter.

*2)* A 32-bit nanoseconds counter. Note that since $10^9$ = 0x3B9ACA00, only 30 bits of this counter actually count.

*3)* A 32-bit fractional nanoseconds counter (LSbit = $2^{-32}$ns).

4) A programmable increment sufficient to add the correct amount of nanoseconds and fractional nanoseconds to the counter each reference clock cycle. (For example, if you are running on a 200MHz clock, the increment should nominally be 5ns per cycle; hence only 3 nanosecond bits and 32 fractional nanosecond bits are required.)

**Note:** All of the PTP counters can be adjusted on-the-fly (setting, adding, and subtracting).

For the ingress, timestamping accuracy in the AQR107-AQR109 is rounded to 16 fractional nanosecond bits (48 + 32 + 16 = 96 bits). This timestamp is appended to the packet (or placed in the packet preamble when operating in USXGMII mode) and the packet's header and FCS are altered accordingly.

The packet can then be passed to the system interface, or placed in a 512 byte FIFO that can be accessed from the MDIO registers space. A similar FIFO in the egress direction supports the ability to send sync packets into the data stream. Note that the MACsec buffers and associated MACS must be operating for this to work.

In order to support asymmetry between the TX and RX path, the AQR107-AQR109 supports a correction register to offset the timestamps by the required amount.

The AQR107-AQR109 also supports the following PTP features:

1) Running the PTP clocks from the received line clock.

2) Running the PTP clocks from an external (up to) 100MHz LVDS clock input.

3) Transparent clock mode.

# Hardware Interfaces† 2

## 2.1 Management Interface

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Interrupt* | INT_N | L8 | OD | The open-drain interrupt signal of the AQR107-AQR109. On reset, this is set high.<br>This output has a 12mA pull-up associated with it. |
| MDIO Address | ADDR0, ADDR1, ADDR2 | F8, M7, K8 | I | The logic inputs for setting the MDIO PHY address of the AQR107-AQR109.<br>This input has a pull-up associated with it. |
| MDIO Clock | MDC | J8 | I | The MDIO clock input for the AQR107-AQR109.<br>This input has a pull-up associated with it. |
| MDIO Data | MDIO | H8 | I/O | This is the MDIO data line for the AQR107-AQR109 with Schmitt-triggered logic levels. On reset, it is set to high-impedance.<br>This is a 12mA I/O. |
| Reset Out* | RST_OUT_N | K3 | OD | The open-drain reset output from the AQR107-AQR109. This may be used to drive the power-up reset signal for a board, as it outputs the on-chip power-up reset signal from the AQR107-AQR109.<br>This output has a 12mA pull-up associated with it. |

*Table 2.1* **Management Interface Signals**

† Table Conventions: any signal name that ends with "*" or pin name that ends with "_N" are active low.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Reset* | RST_N | F3 | I | This is the hard reset input for the AQR107-AQR109 with Schmitt-triggered logic levels.<br>This input has a pull-up associated with it. |
| VDD IO Select | MDIO_1P8_ SELECT_N | H3 | I | When pulled low, this signal enables the I/O to operate from a VDD_IO at 1.8V. When pulled high, the I/O are set to operate at 3.3V.<br>This input has a pull-up associated with it. |

*Table 2.1* **Management Interface Signals** (continued)

The management interface on the AQR107-AQR109 is a two wire interface with a unidirectional MDC clock and a bidirectional MDIO data. The MDIO interface on the AQR107-AQR109 is a robust implementation of this standard. It is designed to operate up to 10.5MHz† and is capable of withstanding voltages up to double the operating voltage (being the theoretical worst-case maximum reflection on an unterminated bus). It utilizes a Schmitt-trigger in conjunction with a debounce state machine to debounce the signals, and is capable of hot-insertion.

The data line is capable of pulling low a 280Ω load tied to 1.8V, and it may be configured to support either open-drain, or push-pull operation in "Global General Provisioning 2: Address 1E.C441". Push-pull is the default operating mode.

In order to provide flexibility to the implementation, the AQR107-AQR109 uses a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% of VDD_IO for $V_{IH}/V_{OH}$ and $V_{IL}/V_{OL}$ respectively. The VDD_IO voltage level affects MDC, MDIO, INT_N, and RST_N. When the VDD_IO is set for 1.8V operation, the pin MDIO_1P8_SELECT_N has to be pulled to ground. When the VDD_IO is set for operation at 3.3V the pin MDIO_1P8_SELECT_N has to be pulled to VDD_IO.

The management interface allows for communication between the Station Management (STA) and a physical layer device (PHY). The STA is the external host controller that is the master of the management interface bus. Consequently, it always sources the MDC clock. When the MDIO is sourced by the STA, the PHY samples the MDIO at the rising edge of MDC. When the MDIO is sourced by the PHY during read operations, the STA samples the MDIO at the rising edge.

† This is a function of whether the output is set to push-pull or open-drain mode, and on the capacitance of the bus.

Table 2.2 shows the management interface frame format (802.3-2005 45.3), and the fields are described as follows:

| Frame | PRE | ST | OP | PHYAD | MMDAD | TA | Data | IDLE |
|---|---|---|---|---|---|---|---|---|
| Address | 1...1 | 00 | 00 | PPPPP | EEEEE | 10 | AAAAAAAAAAAAAAAA | Z |
| Write | 1...1 | 00 | 01 | PPPPP | EEEEE | 10 | DDDDDDDDDDDDDDDD | Z |
| Read | 1...1 | 00 | 11 | PPPPP | EEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |
| Post-read increment address | 1...1 | 00 | 10 | PPPPP | EEEEE | Z0 | DDDDDDDDDDDDDDDD | Z |

*Table 2.2* **MDIO Frame Format**

### 2.1.1 IDLE (Idle Condition)

The idle condition on the management interface is a high-impedance state. All tri-state drivers are disabled and the pull-up resistor(s) on the MDIO bus will pull the MDIO line to a one.

### 2.1.2 PRE (Preamble)

#### 2.1.2.1 Normal Operation

At the beginning of each transaction, the station management entity will send a sequence of 32 contiguous ones on the MDIO data line, along with 32 corresponding cycles on the MDC to provide the MMD with a pattern that it can use to establish synchronization. Each MMD will observe a sequence of 32 contiguous one bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

#### 2.1.2.2 Preamble Suppression

The MDIO interface can optionally disable preamble detection by setting the "MDIO Preamble Detection Disable" bit in "Global General Provisioning 2: Address 1E.C441". In this mode of operation, one or more preamble bit are required followed by the 0x0 start of frame ST bits.

### 2.1.3 ST (Start Of Frame)

The start of frame for indirect access cycles is indicated by the <00> pattern. This pattern assures a transition from the default one and identifies the frame as an indirect access. Frames that contain the ST=<01> pattern defined in Clause 22 are ignored by the MMDs within the AQR107-AQR109.

### 2.1.4 OP (Operation Code)

The operation code field indicates the type of transaction that is being performed by the frame: a <00> pattern indicates that the frame payload contains the address of the register to access, a <01> pattern indicates that the frame payload contains data to be written to the register whose address was provided in the previous address frame, a <11> pattern indicates that the frame is read operation, and a <10> pattern indicates that the frame is a post-read increment address operation.

### 2.1.5 PHYAD (PHY Address)

The PHY address is three bits, which allows for 8 unique PHY addresses, and hence up to 8 PHYs on an MDIO bus (the address of the PHY is determined from the ADDR[2:0] pins; ADDR0, ADDR1, and ADDR2).

The first PHY address bit to be transmitted and received is the Most Significant Bit (MSB) of the address. The station management entity must have *apriori* knowledge of the appropriate PHY address for each PHY to which it is attached, regardless if it is connected to a single PHY or to multiple PHYs.

### 2.1.6 MMDAD (MMD Address)

The MMD address is three bits, which allows for 8 unique MMDs per PHY. The first MMD address bit transmitted and received is the MSB of the address. In addition, the AQR107-AQR109 supports a broadcast mode when the PHYAD is 0x00. Only the write and load address opcodes are supported in broadcast mode.

Read and post-read increment opcodes are ignored in broadcast mode. This mode of operation can be enabled via the "MDIO Broadcast Mode Enable"bits ("Global General Provisioning 2: Address 1E.C441").

### 2.1.7 TA (Turnaround)

The turnaround time is a 2-bit time spacing between the MMD address field and the data field of a management frame to avoid contention during a read transaction. For a read or post-read increment address transaction, both STA and the MMD remain in a high-impedance state for the first bit time of the turnaround.

The MMD then drives a zero bit during the second bit time of the turnaround of a read or post-read increment address transaction. During a write or address transaction, the STA transmits a one for the first bit time of the turnaround and a zero for the second bit time of the turnaround, and this behavior is shown in Figure 2.1.

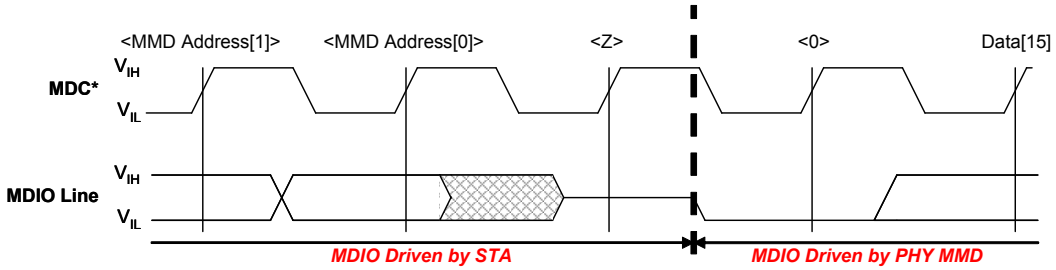


*Figure 2.1* **MDIO Bus Turn-Around During Read Operations**

### 2.1.8 ADDRESS/DATA

The address/data field is 16 bits. For an address cycle, it contains the address of the register to be accessed on the next cycle. For the data cycle of a write frame, the field contains the data to be written to the register. For a read or post-read increment address frame, the field contains the contents of the register. The first bit transmitted and received shall be bit 15.

For counters that are greater than 16-bits, the Least Significant Word (LSW) must be read first, then the MSW must be read immediately afterwards. When the LSW is read, the counter is cleared and the MSW is stored in a shadow register. Reading the MSW actually reads the shadow register. Optionally the host may read the MSW first, then the LSW immediately afterwards by setting the "MDIO Read MSW First Enable" bit in "Global General Provisioning 2: Address 1E.C441".

### 2.1.9 Interrupt

The AQR107-AQR109 supports an open-drain interrupt pin per PHY.

### 2.1.10 Reset

The AQR107-AQR109 supports an active-low reset input. In addition to this, the AQR107-AQR109 is capable of generating a RST_OUT_N signal from its internal power-on reset generation circuitry that can be used by the external board circuitry. Operation of the reset machinery is as follows:

*1)* Release from the Reset state begins when the RST_N input is high†, and all of the core power supplies are above their required thresholds. These thresholds are listed in Table 2.3.

**Note:** Typically, power-on reset thresholds are 20% below the nominal value for analog DC power supplies. For example, for VA21 >1.68V nominal

† Note that there are no timing requirements on issuance of reset relative to the clock

| Supply | Parameter | Min | Max | Units |
|---|---|---|---|---|
| VA21 | Power-on reset threshold for VA21 DC supply | 1.70 | 1.80 | V |
| VA12 | Power-on reset threshold for VA12 DC supply | 0.93 | 0.99 | V |
| VDD | Power-on reset threshold for VDD DC supply | 0.56 | 0.60 | V |

*Table 2.3* **Power-On Reset Thresholds for Core Supply Voltages**

threshold value and for VA12 >0.96V nominal threshold value.

*2)* Once all of the conditions for release from Reset are true, a 20ms timer engages, the purpose of which is to allow the supplies to settle prior to allowing the PHY to boot.

*3)* After the 20ms timer has completed, hardware state machines designed to guarantee PLL and band-gap stability engage.

*4)* After the PLLs and band-gap are locked and functioning properly, the processor and digital circuitry are released from reset.

*5)* The PHY image is then loaded through MDIO boot-load and the processor boots.

*6)* After the processor boots, any provisioned register values are set, and the PHY enters the provisioned operating state.

*7)* Once this is complete, the processor raises the MMD reset bits and sets the Reset Completed alarm, indicating it has completed reset and is ready for operation.

### 2.1.11 Configuration

The AQR107-AQR109 contains a number of static configuration pins that are used to set the power-up operation of the AQR107-AQR109, and these signals include:

*1)* MDIO Address (ADDR[2:0])

## 2.2 Serial FLASH

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| SPI Chip Enable* | CE_N | F2 | O | The SPI CE* signal from the AQR107-AQR109 to the serial FLASH. On reset, this is set high.<br>This is a 12mA output and has a pull-up associated with it. |
| SPI Serial Clock | SCLK | E1 | O | The SPI clock from the AQR107-AQR109 to the serial FLASH. On reset, this is set low.<br>This is a 12mA output and has a pull-down associated with it. |
| SPI Serial Input Data | SIN | D1 | I | Clock signal for slave SMBus used for debug port into PHY MDIO register space. This signal requires a pull-up to VDD_IO.<br>This input has a pull-up associated with it. |
| SPI Serial Output Data | SOUT | F1 | O | The SPI output data from the AQR107-AQR109 to the serial FLASH. On reset, this is set low.<br>This is a 12mA output and has a pull-down associated with it. |

*Table 2.4* **Serial FLASH Signals**

The AQR107-AQR109 is capable of two modes of boot operation:

*1)* MDIO boot-load

*2)* Daisy Chain master

When functioning in Daisy Chain master mode, the AQR107-AQR109 has an attached SPI FLASH, and the PHY's firmware image is loaded from the FLASH. Integrity checking of the loaded image is performed in hardware via a CRC embedded in the image, and if there is an error, a reload is automatically requested. When functioning in MDIO boot-load mode, no FLASH device is required.

Instead, the firmware image is loaded via the MDIO interface, and integrity checking of the loaded image is performed via a hardware CRC function on the memory interface. In order to use MDIO boot-load, the boot-load functions from the API should be carefully studied, or used verbatim.

### 2.2.1 SPI FLASH Interface

The SPI interface is responsible for connecting the AQR107-AQR109 to the external FLASH memory device. The microcontroller on the AQR107-AQR109 accesses the boot code and AQR107-AQR109 default register values from the FLASH memory after power-on reset. This FLASH memory is also accessible via the MDIO interface for firmware updates and manufacturing burn via the API, or via the registers in the Global MMD.

The SPI interface is a four-wire, unidirectional, serial bus as shown in Figure 2.2, and is composed of the following: a serial clock output “SCLK”, a serial data output “SOUT”, a chip-select “CE*” (all the signals are unidirectional), and a a serial data input “SIN”.

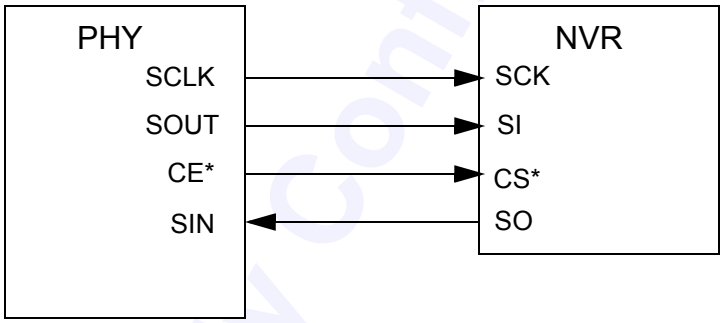


*Figure 2.2* **SPI Interface Block Diagram**

The AQR107-AQR109 is set up to function as a Mode 0 (0,0) SPI device, which means that the clock defaults to zero when not bursting. Data on this interface, for both SIN and SOUT, is always sourced on the falling edge of SCLK, and sampled on the rising edge of SCLK.

Figure 2.3, Figure 2.4, and Figure 2.5 show typical read, burst read, and write operations for the AQR107-AQR109. In all of these scenarios, use the API or the NVR interface in the Global MMD to access the FLASH.

The NVR interface in the AQR107-AQR109 is designed to be able to output any arbitrary opcode, followed by a programmable zero to three address bytes, which is followed by a programmable zero to four data bytes.

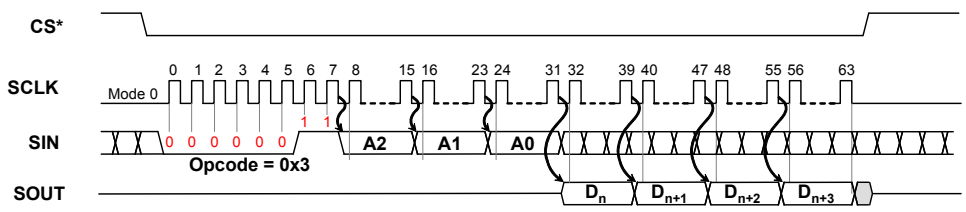


*Figure 2.3* **SPI Read**

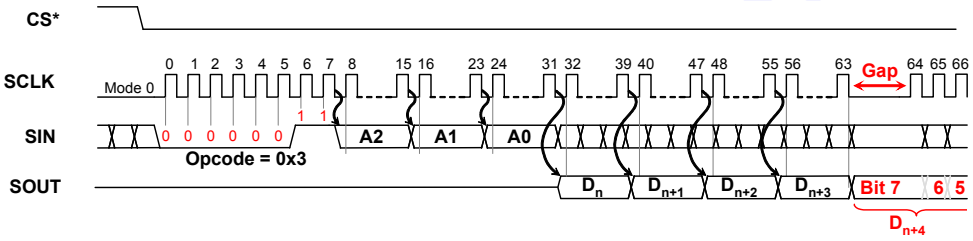


*Figure 2.4* **SPI Burst Read**

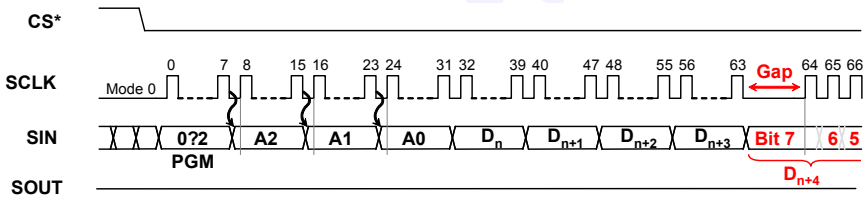


*Figure 2.5* **SPI Burst Write**

This allows any variation of opcodes to be output to the attached FLASH device. This interface also supports a burst read and write mode, which keeps the CS* line pulled low to enable back-to-back reads and writes.

To support this, the NVR interface supports two 16-bit address registers and two 16-bit data registers, which allows up to 4 data bytes in a burst over the SPI interface. To extend this to longer bursts, the AQR107-AQR109 halts the clock after the last bit in the data burst allowing the host processor to load another block of data *to/from* the NVR interface.

This is shown in Figures 2.4 and 2.5 and allows the data burst to be extended by as many bytes as necessary, without outstripping the MDIO's I/O capabilities. Note that typical NVRs require that writing be performed on a block basis, and thus the addresses usually wrap within the block being programmed. As such, it is desirable from a speed and efficiency perspective to attempt to write entire blocks, versus pieces of blocks.

In order to assure that no polling is required on NVR interface, it is recommended that the NVR clock speed be set to at least†:

$$f_{SCLK} > \frac{64}{63} \cdot f_{MDIO}$$

The desired FLASH memory should be chosen to be at least 512K bytes in size

### 2.2.2 Boot-Load

Regardless if the PHY is a daisy-chain master, new images can be boot-loaded into the PHY's IRAM and DRAM via the MDIO interface. In addition, if a boot-load operation is desired as the product's standard operating mode, the FLASH can be depopulated, and the image always loaded on power-up. For more information on this mode of operation, please refer to the API documentation.

## 2.3 Firmware

The AQR107-AQR109 contains a 32-bit microcontroller, and this microcontroller is designed to have its IRAM and DRAM either loaded on power-up/reset from the attached FLASH, via the daisy-chain loading described in Section 2.2, or to have its boot image loaded by the host processor via the MDIO interface. Programming of the FLASH on the daisy-chain master device is done via the appropriate function in the API.

### 2.3.1 Provisionable Default

Another feature of the AQR107-AQR109 is the ability to change and store the default values of any field marked as "PD". A delta list of all defaults that are different from the hardware defaults are stored in the image, and upon power-up, the PHY's microprocessor overwrites the hardware defaults with these new values.

Provisioning new default values is done using the Aquantia Default Provisioning tool, and PHYs are identified by hop count, allowing each PHY to be uniquely provisioned.

### 2.3.2 Gang-Load

In order to save time on MDIO boot-loading operations, the AQR107-AQR109 supports a gang-load feature, whereby multiple AQR107-AQR109 chips on a single MDIO bus may be simultaneously loaded with boot images.

† This is derived from the fact that the longest burst instruction on the SPI is 64 bits, at one bit per clock, whereas to write a register on the MDIO takes 64 clocks, and the data is not written until the last bit - hence the 63.

This is done by temporarily setting all of the device's MDIO addresses to be the same, loading the boot image, and then toggling the MDIO Address Reset bit in the Global register MMD.

This can also be handled using the API (for specific details, refer to the API documentation). One additional option is to enable MDIO broadcast on address 0.

## 2.4 SerDes

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Lane 0 RX | RX_P, RX_N | N2, N3 | I | PHY 0 Physical Lane 0 differential RX of the AQR107-AQR109 SerDes interface. This lane can operate in KR, 2500BASE-X, and SGMII mode. |
| Lane 0 TX | TX_P, TX_N | N6, N5 | O | PHY 0 Physical Lane 0 differential TX of the AQR107-AQR109 SerDes interface. This lane can operate in KR, 2500BASE-X, and SGMII mode. |

*Table 2.5* **SerDes Signals**

The AQR107-AQR109 SerDes interface is both robust and flexible, and provides numerous loopback and diagnostic capabilities which ease system interface-PHY board design and bring-up, as well as AC JTAG. The interface is capable of providing arbitrary lane swapping and inversion.

In the transmit direction, there is a programmable 3 tap equalizer (1 precursor tap and 1 postcursor tap), as well as the ability to program the TX drive strength, and TX termination. In the receive direction, there is programmable gain and programmable boost. The SerDes interface on the AQR107-AQR109 also contains diagnostic pattern generation and checking functionality that is listed in the subsequent sections.

Another feature that the AQR107-AQR109 SerDes interface can provide is the eye-diagram mode, which allows the user to create an eye-diagram. To use this functionality, the appropriate API functions must be called.

All of the parameters associated with the SerDes interface have provisionable default values, which means that the AQR107-AQR109 SerDes interface can be tailored to power-up with the optimal settings for any given application.

| Test | Description | Generate | Check | Invert |
|---|---|---|---|---|
| $x^9$ PRBS | $x^9 + x^5 + 1$ | X | X | X |
| $x^{31}$ PRBS | $x^{31} + x^{28} + 1$ | X | X | X |
| Square Wave | Clause 49.2.12 | X | X | X |
| Pseudo-Noise | | X | X | X |
| CRPAT | IEEE 802.3 Annex48A.4 | X | X | X |

*Table 2.6* **KR Diagnostic Pattern Capabilities**

| Test | Description | Generate | Check | Invert |
|---|---|---|---|---|
| CRPAT | IEEE 802.3 Annex48A.4 | X | X | X |

*Table 2.7* **SGMII Diagnostic Pattern Capabilities**

## 2.5 SerDes System I/F Start-Up

In start-up on the system interface side, there are four different operating scenarios for the SerDes I/F:

*a)* 10G mode (KR / XFI)

*b)* 2500BASE-X mode

*c)* 1000BASE-X mode

*d)* XSGMII mode†

*e)* All-off mode

These different modes affect only the system interface, and function independently of whether the MDI or KR-look-aside interface is selected.

### 2.5.1 10G Mode

*1)* In this mode, which is the hardware default, the AQR107-AQR109 comes up in the pre-configured 10G mode (KR/XFI) and transmits Local

† XSGMII is an extension of the Cisco SGMII protocol which informs the system interface what the PHY has autonegotiated as a rate. The XSGMII extension as proposed by Aquantia uses this same mechanism, but also informs of a 10G connection. After receiving acknowledgment of a 10G connection, the PHY switches to the pre-configured 10G mode. For more details see XSGMII on page 90.

Faults/Idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the AQR107-AQR109 stays in the pre-configured 10G mode, 1000BASE-X mode, or 100M SGMII mode depending on the autonegotiated line rate.

3) Once the SerDes I/F has synchronized, traffic flows.

4) If the link fails and the system interface was in the 10G mode, the AQR107-AQR109 generates a Local Fault message towards the system I/F, effectively restarting. If the link had transitioned to 1G operation, the SerDes is restarted in 10G mode generating Local Faults/Idles.

5) Autonegotiation restarts after the link break timer expires.

### 2.5.2 2500BASE-X Mode

1) In this mode, the AQR107-AQR109 comes up in 2500BASE-X mode and transmits idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the AQR107-AQR109 either stays in 2500BASE-X mode, or switches to the pre-configured 10G mode, or 1G/100M SGMII mode depending on what the autonegotiated line rate was.

3) Once the SerDes I/F has synchronized, traffic flows.

4) If the link fails and the system interface was in the pre-configured 10G mode (KR/XFI), the AQR107-AQR109 generates a Local Fault message towards the system I/F, and effectively restarts in 2500BASE-X mode, generating Idles. Otherwise, the link remains in 2500BASE-X mode and continues generating Idles.

5) Autonegotiation restarts after the link break timer expires.

### 2.5.3 1000BASE-X Mode

1) In this mode, the AQR107-AQR109 comes up in 1000BASE-X mode and transmits idles, and remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the AQR107-AQR109 either stays in 1000BASE-X mode, switches to the

pre-configured 10G mode or to the 100M SGMII mode depending upon what was the autonegotiated line rate.

3) Once the SerDes I/F has synchronized, traffic flows.

4) If the link fails and the system interface was in the pre-configured 10G mode (KR/XFI) AQR107-AQR109 generates a Local Fault message towards the system I/F, and effectively restarts in 1000BASE-X mode, generating Idles. Otherwise, the link just stays in 1000BASE-X mode generating Idles.

5) Autonegotiation restarts after the link break timer expires.

### 2.5.4 XSGMII Mode

1) In this mode, the AQR107-AQR109 comes up in XSGMII mode. After sending and receiving an ACK on an XSGMII link-down autonegotiation message (for more information, see Table 2.8), the SerDes transmits Idles, and it remains in this state until a connection to a link partner is established.

2) After a connection to a link partner has been established, the AQR107-AQR109 sends an XSGMII Link Up autonegotiation message with the appropriate rate† (see Table 2.8), and receives an ACK.

3) Upon receiving the acknowledge from the system interface, the AQR107-AQR109 either switches to 100M SGMII mode, stays in 1G SGMII mode (essentially 1000BASE-X), or switches to the pre-configured 10G mode (KR/XFI/USXGMII), depending on whether the autonegotiated line rate was 1G/100M or 10G.

4) Once the SerDes I/F has synchronized, traffic flows.

5) If the link fails, and the AQR107-AQR109 was in the pre-configured 10G mode, the AQR107-AQR109 generates a Local Fault message towards the system I/F, and then transitions back to XSGMII mode. It then sends and receives an ACK on an XSGMII link-down autonegotiation message, and then resumes transmitting Idles.

† The SGMII autonegotiation machinery was derived from 1000BASE-X and involves exchanging 16-bit control words via /C and /I ordered sets. It was adopted for SGMII to solve the issue of how a copper SFP module would inform the system interface what rate it had autonegotiated on the line, without having an MDIO interface (SFP-only support).

If the link fails and the AQR107-AQR109 was in 1G SGMII mode, the AQR107-AQR109 first sends and receives an ACK on an XSGMII link-down autonegotiation message, and then resumes transmitting Idles, with no interruption in SerDes operations.

If the system I/F was in 100M SGMII mode, the SerDes transitions back to XSGMII mode, where it sends and receives an ACK on an XSGMII link-down autonegotiation message, and then resumes transmitting Idles.

*6)* Autonegotiation restarts after the link break timer expires.

### 2.5.5 USXGMII Mode

*1)* In this mode, the AQR107-AQR109 comes up in USXGMII mode. After sending and receiving an ACK on an USXGMII link-down autonegotiation message (for more information, see Table 2.9), the SerDes transmits Idles, and remains in this state until a connection to a link partner is established.

*2)* After a connection to a link partner has been established, the AQR107-AQR109 sends an USXGMII Link Up autonegotiation message with the appropriate rate† (see Table 2.9), and receives an ACK.

*3)* Upon receiving the acknowledge from the system interface, the AQR107-AQR109 switches to the desired rate, depending on whether the autonegotiated line rate was 100M, 1G, 2.5G, 5G, or 10G.

*4)* Once the SerDes I/F has synchronized, traffic flows.

† The SGMII autonegotiation machinery was derived from 1000BASE-X and involves exchanging 16-bit control words via /C and /I ordered sets. It was adopted for SGMII to solve the issue of how a copper SFP module would inform the system interface what rate it had autonegotiated on the line, without having an MDIO interface (SFP-only support).

5) If the link fails, the AQR107-AQR109 generates a Local Fault message towards the system I/F, and then transitions back to USXGMII Idle mode, where it sends and receives an ACK on an USXGMII link-down autonegotiation message, and then resumes transmitting Idles.

6) Autonegotiation restarts after the link break timer expires.

### 2.5.6 All-Off Mode

1) In this mode, the AQR107-AQR109 comes up with the system interface off, and remains in this state until a connection to a link partner is established.

2) After connection to a link partner has been established, the AQR107-AQR109 either turns on the pre-configured 10G mode (XFI/KR), 2500BASE-X, 1000BASE-X, or 100M SGMII mode, depending on what the autonegotiated line rate was.

3) Once the SerDes I/F has synchronized, traffic flows.

4) If the link fails and was in the pre-configured 10G mode, the AQR107-AQR109 generates a Local Fault message towards the system I/F, and then shuts off. Otherwise, the system interface just shuts off.

5) Autonegotiation restarts after the link break timer expires.

### 2.5.7 Interrupts

In all of these modes, the processor has the ability to generate an interrupt upon completing autonegotiation.

### 2.5.8 XSGMII

XSGMII is an extension of the SGMII interface and provides the signaling and control for moving to a 10G connection mode in addition to the SGMII rates of 1G, 100M, and 10M.

XSGMII builds upon the existing specification for SGMII, and the existing 10GE specifications defined in 802.3-2005 (for details, see “Serial-GMII Specification Version 1.8“, Document ENG-46158, Cisco Systems, April 27, 2005 on page 591).

The creation of XSGMII requires a minimal change to the existing SGMII specification: namely the addition of a 10G connect rate, as described in the following sequence:

1) System interface and PHY connect and synchronize the SGMII 1.25 Gb/s 8B/10B SerDes link.

2) PHY uses Clause 28 autonegotiation over the MDI to establish a connection with the remote PHY, which is constrained by the abilities the local system interface communicated during step 1, above.

3) PHY uses SGMII (Clause 37) autonegotiation to inform the system interface which rate it is selecting.

4) If a 10G connection is established, after receiving the acknowledgment from the system interface, the PHY switches over to 10G operation and traffic begins to flow after the 10GBASE-T training sequence is completed.

5) If a 100M or 1G connection is established, after receiving the acknowledgment from the system interface, the PHY stays in SGMII mode, and traffic begins to flow after the link is established.

The sequence steps just described require the modifications to Table 1 of the SGMII specification as shown in Table 2.8, with the key modification indicated in red.

| Bit Number | tx_config_Reg[15:0] sent from PHY to System Interface | tx_config_Reg[15:0] sent from System Interface to PHY |
|---|---|---|
| 15 | Link: 1 = link up, 0 = link down | 0: Reserved for future use |
| 14 | Reserved for Auto-Negotiation acknowledge as specified in 802.3z | 1 |
| 13 | 0: Reserved for future use | 0: Reserved for future use |
| 12 | Duplex mode: 1 = full duplex (required) | 0: Reserved for future use |
| 11:10 | Speed: Bit 11, 10<br>**1 1 = 10 Gbps: 10GBASE-T, 10GBASE-R**<br>1 0 = 1000 Mbps: 1000BASE-TX, 1000BASE-X<br>0 1 = 100Mbps: 100BASE-TX, 100BASE-FX<br>0 0 = 10Mbps: 10BASET, 10BASE2, 10BASE5 | 0: Reserved for future use |
| 9:1 | 0: Reserved for future use | 0: Reserved for future use |
| 0 | 0 | 1 |

*Table 2.8* **XSGMII Base Page**

### 2.5.9 USXGMII

USXGMII is an extension of the XFI interface and provides the signaling and control for moving to a 100M, 1G, 2.5G, and 5G connection mode in addition to the XFI rates of 10G. USXGMII builds upon the existing specification for XFI and existing 10GE specifications defined in 802.3-2005 (for details, see “Serial-GMII Specification Version 1.8“, Document ENG-46158, Cisco Systems, April 27, 2005 on page 591).

The creation of USXGMII requires that a minimal change be made to the existing XFI specification; for example, the addition of 100M, 1G, 2.5G, and 5G connection rates as described in the following sequence:

1) System interface and PHY connect and synchronize the XFI 10.3125 Gb/s 64B/66B SerDes link.

2) PHY uses Clause 28 autonegotiation over the MDI to establish a connection with the remote PHY, which is constrained by the abilities the local system interface communicated during step 1, above.

3) PHY uses SGMII (Clause 37) autonegotiation to inform the system interface about the rate it is selecting.

4) If a 10G connection is established, after receiving the acknowledgment from the system interface, the PHY switches over to 10G operation and traffic begins to flow after the 10GBASE-T training sequence is completed.

5) If a 100M, 1G, 2.5G, or 5G connection is established, after receiving the acknowledgment from the system interface, the PHY stays in SGMII mode and traffic begins to flow after the link is established.

Table 2.9 on page 93 shows the USXGMII Base Page.

## 2.6 MDI

In 10G mode, the line interface on the AQR107-AQR109 is capable of driving up to 100 meters of Cat 6a unshielded twisted pair or 100 meters of Cat 7 shielded cable (100 Ω differential impedance). It can also drive 55 meters of Cat 6 cable, and a lesser distance of Cat 5e cable†. In 2.5G and 5G modes, it can drive 100 meters of Cat 5e (or better) cable.

† This distance is indeterminate because Cat 5e cable performance is not specified past 100MHz (for details, see “Information Technology - Generic cabling for customer premises”, ISO/IEC 11801, Second edition 2002-09 on page 591).

| Bit Number | usxgmiiChannelInfo[15:0] sent from PHY to System Interface | usxgmiiChannelInfo[15:0] sent from System Interface to PHY |
|---|---|---|
| 15 | Link: 1 = link up, 0 = link down | 0: Reserved for future use |
| 14 | Reserved for Auto-Negotiation acknowledge | 1 |
| 13 | 0: Reserved for future use | 0: Reserved for future use |
| 12 | Duplex mode: 1 = full duplex (required) 0 = half duplex | 0: Reserved for future use |
| 11:9 | Speed: Bit 11, 10, 9<br>0 0 0 = 10Mbps: 10BASET, 10BASE2, 10BASE5<br>0 0 1 = 100Mbps: 100BASE-TX, 100BASE-FX<br>0 1 0 = 1000 Mbps: 1000BASE-TX, 1000BASE-X<br>0 1 1 = 10 Gbps: 10GBASE-T, 10GBASE-R<br>1 0 0 = 2500 Mbps: AQrate 2.5G<br>1 0 1 = 5000 Mbps: AQrate 5G<br>1 1 0 = Reserved<br>1 1 1 = Reserved | 0: Reserved for future use |
| 8 | EEE capability: 1= supported, 0 = not supported | 0: Reserved for future use |
| 7 | EEE clock stop capability: 1= supported, 0 = not supported | 0: Reserved for future use |
| 6:1 | 0: Reserved for future use | 0: Reserved for future use |
| 0 | 1 = USXGMII supported device | 1 |

*Table 2.9* **USXGMII Base Page**

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Pair A | A_P, A_N | C1, B1 | I/O | PHY 0 Pair A of the AQR107-AQR109 line interface. These should connect to the Pair A inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.<br>This is a 4mA I/O. |

*Table 2.10* **MDI Signals**

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Pair B | B_P, B_N | A2, A3 | I/O | PHY 0 Pair B of the AQR107-AQR109 line interface. These should connect to the Pair B inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.<br>This is a 4mA I/O. |
| Pair C | C_P, C_N | A6, A5 | I/O | PHY 0 Pair C of the AQR107-AQR109 line interface. These should connect to the Pair C inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.<br>This is a 4mA I/O. |
| Pair D | D_P, D_N | A8, B8 | I/O | PHY 0 Pair D of the AQR107-AQR109 line interface. These should connect to the Pair D inputs of the transformer, with capacitive bypassing via the center-tap. On reset, this is set to high-impedance.<br>This is a 4mA I/O. |

*Table 2.10* **MDI Signals** (continued)

In 1G and 100M modes, it can drive 130 meters of Cat 5e (or better) cable. It is designed to drive this via a quad, 50Ω, center-tapped 1:1 transformer connected to an RJ-45 PCB-mount jack.

The line interface on the AQR107-AQR109 supports automatic A/B and C/D pair swaps, polarity inversions, auto-X (MDI versus MDI-x operations), and semi-cross (A/B or C/D only). It also supports provisionable ABCD to DCBA pair reversal for ease of routing with stack-jacks via bit 1.E400.1:0. Note that this reversal does not swap polarities (thus, A+ maps to D+, etc.).

## 2.7 Timing

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Clock Source Select | XTAL_SELECT_N | K7 | I | This is the 50MHz reference clock source selector for the AQR107-AQR109. When XTAL_SELECT_N is pulled low, the XTAL_I and XTAL_O pins operate in crystal mode; otherwise they operate in LVDS oscillator input mode.<br>This input has a pull-up associated with it. |
| Crystal Input | XTAL_I | E8 | I | This is the 50MHz reference clock input for the AQR107-AQR109. When XTAL_SELECT_N is pulled low, these pins operate in crystal mode. Otherwise, they are the differential LVDS inputs for an external oscillator, with XTAL_I being the positive input and XTAL_O being the negative input. In oscillator mode, this DC-coupled input has an internal 100Ω termination resistor associated with it.<br>This input has a pull-up associated with it. |
| Crystal Output | XTAL_O | D8 | I | This is the 50MHz crystal oscillator output of the AQR107-AQR109. This connects to the output of an inverting amplifier. In XO mode, this is high-impedance.<br>This input has a pull-up associated with it. |

*Table 2.11* **Timing Signals**

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| PTP/1588 Sync | SYNC_1588 | E2 | I | The PTP sync input used to align the PTP clocks on multiple PHYs on a platform to have the same time. The PHY timestamps the rising edge of this input and this timestamp can then be used on each of the PHYs to perform the alignment.<br>This input has a pull-down associated with it. |
| PTP External Clock | CLK_1588_P, CLK_1588_N | H1, G1 | I -LVDS | The PTP differential LVDS clock input. This input has a 100Ω termination associated with it, and will operate in the frequency range of 40MHz to 100MHz. This pin should be AC coupled. |
| Sync-E Primary Clock | CLKO_50M_A | G8 | O | The primary recovered clock output used for synchronous Ethernet (Sync-E).<br>This output and has a 12mA pull-down associated with it. |

*Table 2.11* **Timing Signals** (continued)

The AQR107-AQR109 contains a high-performance synthesizer that is capable of producing all of the clocks required internally, as well as sourcing the recovered 50MHz CMOS clock for use by other components in the system.

This synthesizer operates from either an external 100µW 50.000MHz crystal or from a differential 50MHz clock. The 50MHz CMOS clock output is synchronized to the recovered clock, and is thus capable of being used in a synchronous Ethernet application. Enabling of this is done via the Global MMD.

## 2.8 LED

The AQR107-AQR109 supports three 20mA, open-drain CMOS LED outputs (see Table 2.12). Configuration of the LEDs is done via the API.

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| LED [2:0] | LED0, LED1, LED2 | H2, G2, G3 | O | LED0 output for PHY 0. These lines sense whether the LED is pulled high or low and drive accordingly. The configuration state of the LEDs is visible in the register space. On reset, these pins are set to high impedance.<br>This is a 20mA output and has a pull-up associated with it. |

*Table 2.12* **LED Signals**

## 2.9 Reference Resistors

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Bandgap Reference Resistor | RREF_BG | B7 | Analog | The connection point for the bandgap reference resistor. This should be a precision 1%, 2.00kΩ resistor tied to ground. |

*Table 2.13* **Reference Resistors Signals**

The AQR107-AQR109 relies on 1% precision resistors to calibrate its internal voltage levels.

## 2.10 JTAG

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| JTAG Clock | TCK | M1 | I | The JTAG clock input.<br>This input has a pull-down associated with it. |
| JTAG Data Input | TDI | L1 | I | The JTAG data input signal.<br>This input has a pull-down associated with it. |
| JTAG Data Output | TDO | K1 | O | The JTAG data output signal.<br>This is a 12mA output and has a pull-down associated with it. |
| JTAG Reset | TRST_N | J3 | I | The JTAG reset signal. If JTAG is not used, this pin *must* be pulled low.<br>This input has a pull-up associated with it. |
| JTAG Test Mode State | TMS | J2 | I | The JTAG test mode state signal.<br>This input has a pull-down associated with it. |

*Table 2.14* **JTAG Signals**

The AQR107-AQR109 supports a IEEE 1149.1 compliant JTAG interface, with 1149.6 AC JTAG support on the SerDes interface. Note that for normal operation, TRST_N should be held low.

## 2.11 Debug

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Slave SMBus | SMB_DAT, SMB_CLK | M8, L7 | I/O | Data signals for slave SMBus used for debug port into PHY MDIO register space and these signals require an external pull-up to VDD_IO.<br>This is a 12mA I/O and it has a pull-up associated with it. |

*Table 2.15* **Debug Signals**

The AQR107-AQR109 supports a side-access port to the MDIO register space via a slave SMBus. Addressing for this SMBus is provisioned on a per PHY basis.

**Note:** It is recommended that every design connect these SMBus pins to a header to allow in-system debug. This obviates the need to disconnect the MDIO lines, and allows for normal system operation during debug.

## 2.12 Power

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| AVDD12 | VA12 | C6, D5 | Power | 1.2V analog supply. |
| AVDD21 | VA21 | C4, D3 | Power | 2.1V analog supply. |
| AVSS | AVSS | A1, A4, A7, B2, B3, B5, B6, C2, C3, C5, C8, D2, D4, D7 | Power | Analog ground. |
| AVSS PLL | AVSS_PLL | B4 | Power | Analog ground for PHY PLL. |
| VCC Crystal | VA21_XTAL | C7 | Power | 2.1V supply for the crystal oscillator. |
| VDD | VDD | G4, G6, H5, H7, J4, J6, L3 | Power | 0.85V digital supply. |
| VDD IO Power Supply | VDD_IO | M6 | Power | The power supply for the general I/O on the AQR107-AQR109. High and low logic levels are scaled to 70% and 30% of the supply voltage, respectively. |
| VDD SERDES | VDD_SRDS | M4 | Power | SerDes 0.85V digital supply. |
| VSS | VSS | G5, G7, H4, H6, J5, K5, L2, L6 | Power | Digital ground. |
| VSS SERDES | VSS_SRDS | M2, M3, M5, N1, N4, N7 | Power | SerDes ground. |

*Table 2.16* **Power Signals**

The AQR107-AQR109 utilizes three separate power supplies to minimize power consumption:

1) VDD

2) 1.2V

3) 2.1V

As mentioned before, to provide flexibility to implementation, the AQR107-AQR109 utilizes a programmable I/O voltage. The logic thresholds for the I/O are set at 70% and 30% of VDD_IO for $V_{IH}/V_{OH}$ and $V_{IL}/V_{OL}$, respectively.

The VDD_IO voltage level affects MDC, MDIO, INT_N, and RST_N:

1) When the VDD_IO is set for 1.8V operation, the MDIO_1P8_SELECT_N pin has to be pulled to ground.

2) When the VDD_IO is set for 3.3V operation, the MDIO_1P8_SELECT_N pin has to be pulled to VDD_IO.

## 2.13 Reserved

| Signal Name | Pin Name(s) | Pin Number(s) | Type | Description |
|---|---|---|---|---|
| Floating | NC | D6, E3, E4, E5, E6, E7, F4, F5, F6, F7, K2, L4, L5 | n/a | These pins are floating in the package and they can be connected as conditions dictate. |
| Reserved No Connect | RNC_K4, RNC_J7, RNC_K6, RNC_J1, RNC_N8 | K4, J7, K6, J1, N8 | n/a | |

*Table 2.17* **Reserved Signals**

## 2.14 Pin-Out

The pin-out for the AQR107-AQR109 is shown in Figure 2.6. The signals are color coded to group similar functionalities together, and the perspective view is looking from the top of the chip.

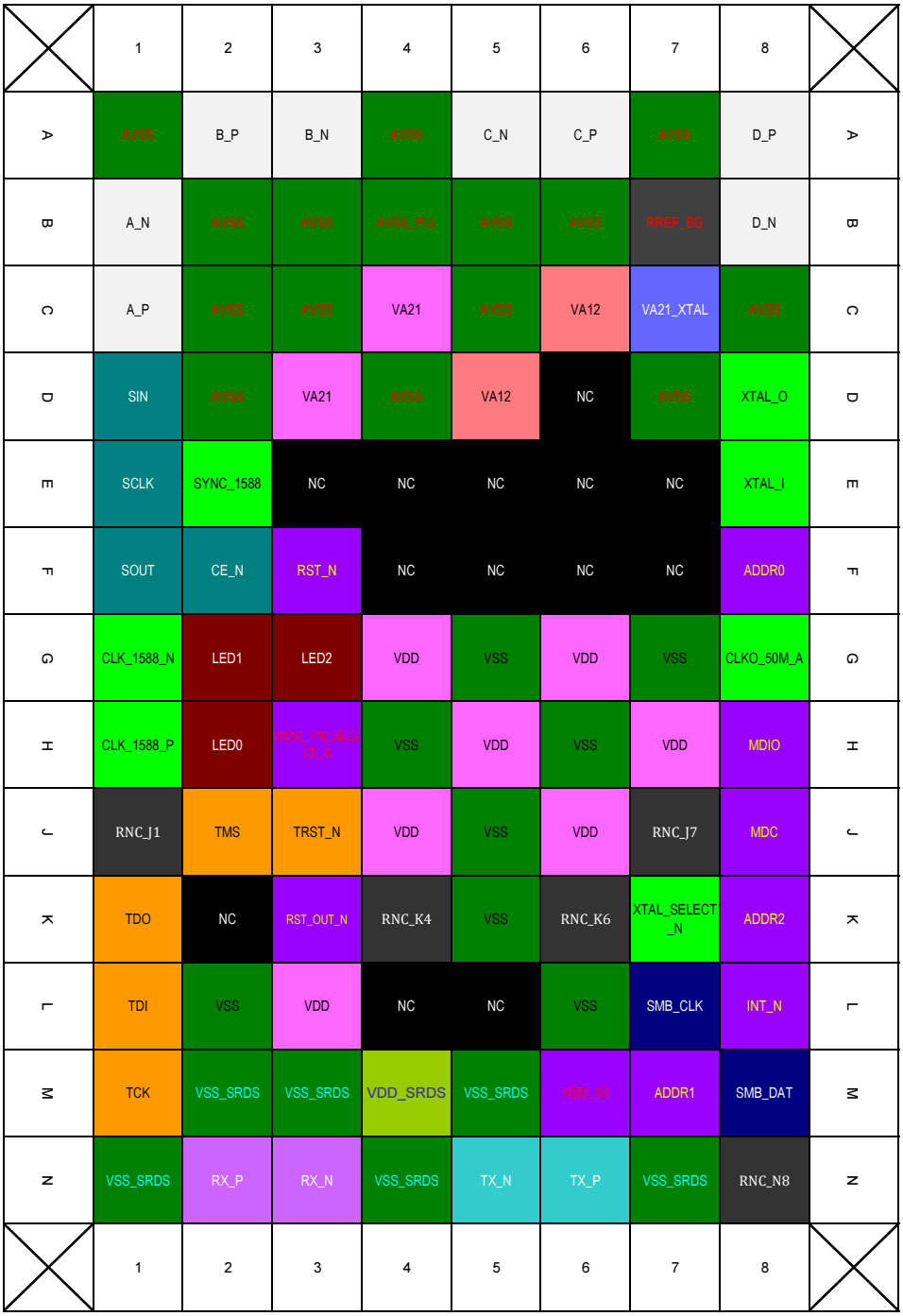


*Figure 2.6* **AQR107-AQR109 Pin-Out**

# Timing 3

## 3.1 MDIO

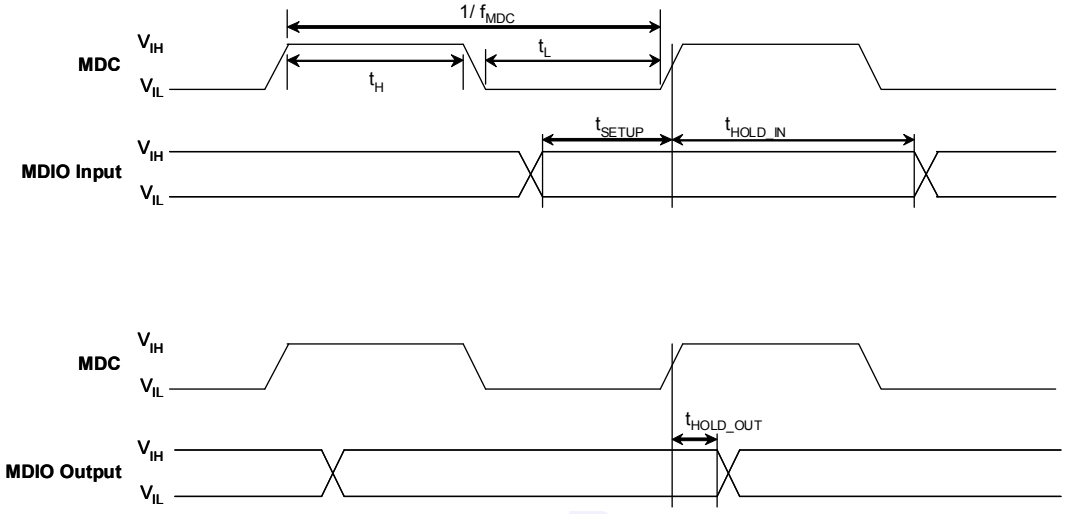


*Figure 3.1* **MDIO Setup and Hold Times**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{MDC}$ | MDC Frequency | | | | 10.5 | MHz |
| $t_L$ | MDC Low Time | | 20 | | | ns |
| $t_H$ | MDC High Time | | 20 | | | ns |
| $t_{SETUP}$ | Input Setup Time | | 8 | | | ns |
| $t_{HOLD\_IN}$ | Input Hold Time | | 10 | | | ns |
| $t_{HOLD\_OUT}$ | Output Hold Time | | 29 | | 38 | ns |

*Table 3.1* **MDIO Timing**

Data is sampled on the rising edge of MDC at the PHY, and at the STA.

## 3.2 Interrupt

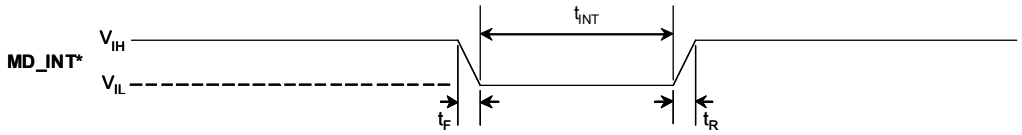


*Figure 3.2* **Interrupt Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_F$ | Fall Time | | 1 | | | ns |
| $t_R$ | Rise Time | | 1 | | | ns |
| $t_{INT}$ | Interrupt Time | | N/A[1] | | | ns |

*Table 3.2* **Interrupt timing**

1. INT* stays low until the interrupt is serviced

## 3.3 Reset

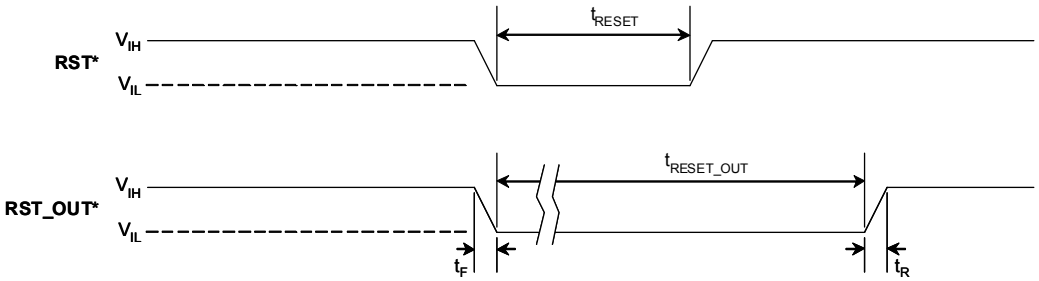


*Figure 3.3* **Reset Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{RESET}$ | Reset Time | | 100 | | | ms |
| $t_F$ | Fall Time | | 1 | | | ns |
| $t_R$ | Rise Time | | 1 | | | ns |
| $t_{RESET\_OUT}$ | Reset Out Time | $f_C$ = 50.00MHz | 20 | | | ms |

*Table 3.3* **Reset Timing**

## 3.4 SPI

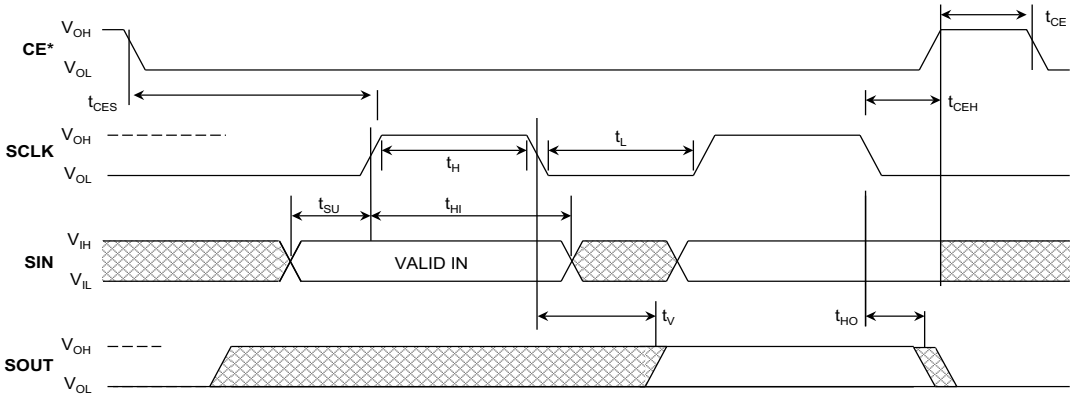


*Figure 3.4* **SPI Timing Diagram**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK Clock Frequency[1] | | 0 | | 50.0 | MHz |
| $t_H$ | SCLK High Time | | 12 | | | ns |
| $t_L$ | SCLK Low Time | | 12 | | | ns |
| $t_{CE}$ | CE* High Time | | 50 | | | ns |
| $t_{CES}$ | CE* Setup Time | | 25 | | | ns |
| $t_{CEH}$ | CE* Hold Time | | 25 | | | ns |
| $t_{SU}$ | $S_{IN}$ Setup Time | | 14 | | | ns |
| $t_{HI}$ | $S_{IN}$ Hold Time | | -4 | | | ns |
| $t_V$ | $S_{OUT}$ Output Valid | | | | 4 | ns |
| $t_{HO}$ | $S_{OUT}$ Hold Time | | -4 | | | ns |

*Table 3.4* **SPI Timing**

1. An attached FLASH device which supports 40MHz operation, must have a $t_V$ (output valid time) of less than 12.5ns.

## 3.5 SerDes

| Maximum Total Jitter ($TJ_{MAX}$) | Maximum Random Jitter ($RJ_{MAX}$) | Maximum Data Dependent Jitter ($DDJ_{MAX}$) | Maximum Deterministic Jitter ($DJ_{MAX}$) | Maximum Periodic Jitter ($PJ_{MAX}$) | Units |
|---|---|---|---|---|---|
| 1.00 | 0.25 | 0.55 | 0.10 | 0.10 | UIpp |

*Table 3.5* **SerDes Receiver Jitter Tolerance Specifications**

| Maximum Total Jitter ($TJ_{MAX}$) | Maximum Random Jitter ($RJ_{MAX}$) | Maximum Deterministic Jitter ($DJ_{MAX}$) | Maximum Periodic Jitter ($PJ_{MAX}$) | Units |
|---|---|---|---|---|
| 0.25 | 0.15 | 0.05 | 0.05 | UIpp |

*Table 3.6* **SerDes Transmit Jitter Tolerance Specifications**

The measurement BW for these specs is from $\frac{f_{\mathrm{SYMBOL}}}{1667}$ to $\infty$, as the tracking bandwidth of the PLL for the SerDes is up to $\frac{f_{\mathrm{SYMBOL}}}{1667}$.

For instance, for KR, the symbol rate is 10.3125GHz, so $\frac{f_{\mathrm{SYMBOL}}}{1667} \cong 6\mathrm{MHZ}$. Thus, the measurement BW for the integrated jitter is from roughly 6MHz to infinity.

## 3.6 SGMII Transmit

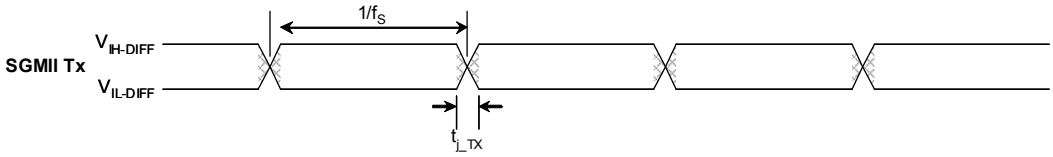


*Figure 3.5* **SGMII Transmit Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_S$ | Symbol Rate | | | 1.25 | | GS/s |

*Table 3.7* **SGMII Transmit Timing**

## 3.7 SGMII Receive

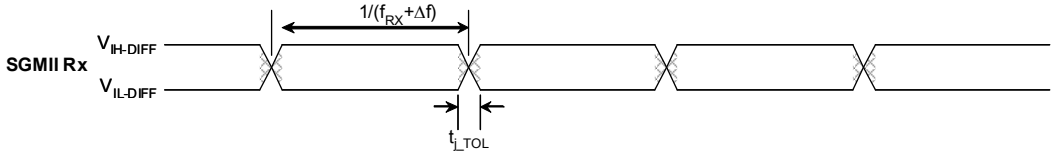


*Figure 3.6* **SGMII Receive Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{RX}$ | Receive Symbol Rate | | | 1.25 | | GS/s |
| $\Delta_f$ | Frequency Tolerance | | -300 | | 300 | ppm |

*Table 3.8* **SGMII Receive Timing**

## 3.8 KR Transmit

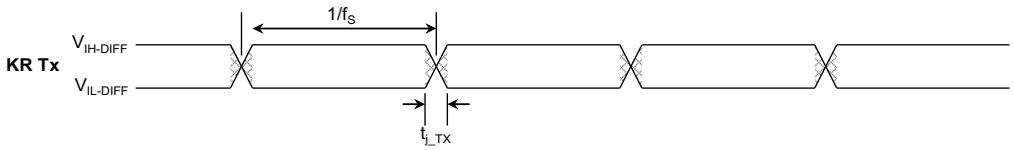


*Figure 3.7* **KR Transmit Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_S$ | Symbol Rate | | | 10.3125 | | GS/s |

*Table 3.9* **KR Transmit Timing**

## 3.9 KR Receive

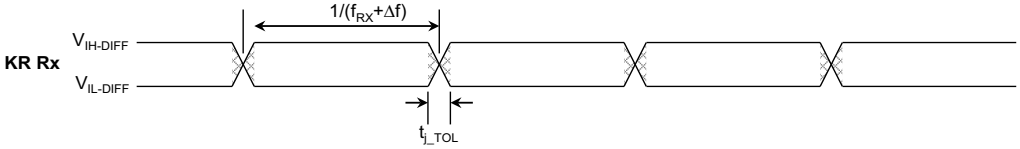


*Figure 3.8* **KR Receive Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{RX}$ | Receive Symbol Rate | | | 10.3125 | | GS/s |
| $\Delta_f$ | Frequency Tolerance | | -50 | | 50 | ppm |

*Table 3.10* **KR Receive Timing**

## 3.10 2500BASE-X Transmit

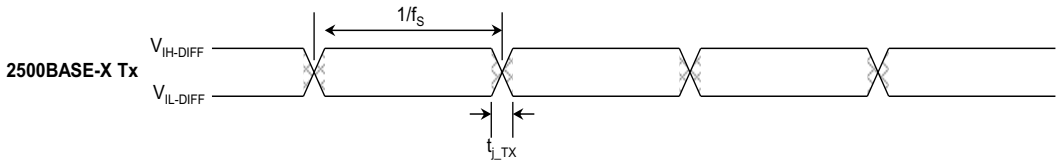


*Figure 3.9* **2500BASE-X Transmit Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_S$ | Symbol Rate | | | 3.125 | | GS/s |

*Table 3.11* **2500BASE-X Transmit Timing**

## 3.11 2500BASE-X Receive

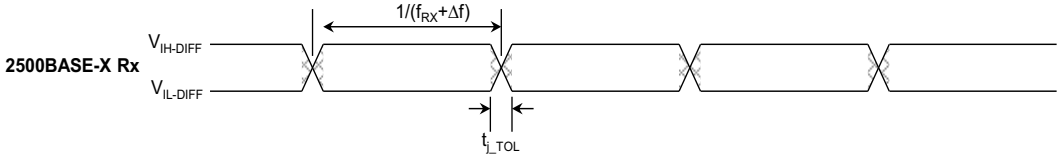


*Figure 3.10* **2500BASE-X Receive Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{RX}$ | Receive Symbol Rate | | | 3.125 | | GS/s |
| $\Delta_f$ | Frequency Tolerance | | -300 | | 300 | ppm |

*Table 3.12* **2500BASE-X Receive Timing**

## 3.12 Clocks

### 3.12.1 Input

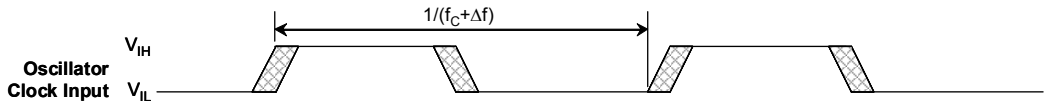


*Figure 3.11* **50MHz Input Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_C$ | Clock Frequency | | | 50.0 | | MHz |
| $\Delta_f$ | Frequency Tolerance | | -50 | | 50 | ppm |
| $t_j$ | RMS Jitter[1] | 12KHz - 20MHz | | | 1.0 | ps |
| DC | Duty Cycle | | 45 | | 55 | % |

*Table 3.13* **50.000MHz Input Timing**

1. This includes all period jitter and tones.

The phase noise of the 50MHz input clock should be at least as good as the mask shown in Figure 3.12:

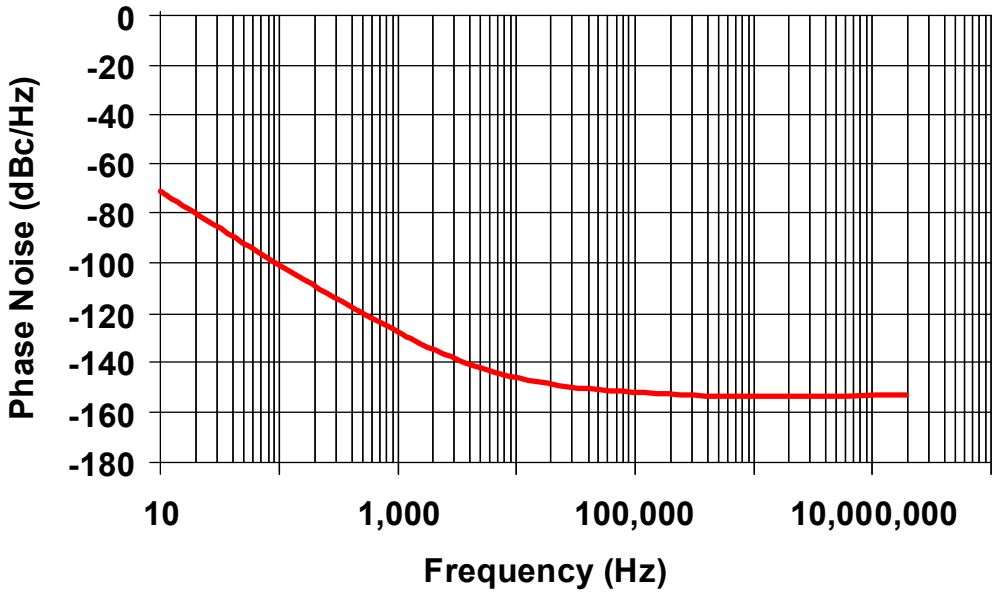


*Figure 3.12* **50.000MHz Phase Noise Mask**

### 3.12.2 Output

The timing information for the AQR107-AQR109 output clock (CLKO_50M_A) are shown in Table 3.14. Note that the 50MHz clock is phase-locked to the incoming receive signal in 1G and 10G slave mode. The result is that their frequency accuracy in these modes is a function of the far-end device's clock accuracy.

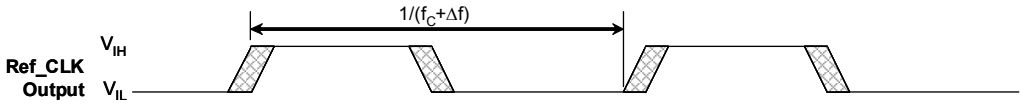


*Figure 3.13* **50MHz Reference Clock Output Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_C$ | Clock Frequency | | | 50.000 | | MHz |
| $\Delta_f$ | Frequency Tolerance | | -50 | | 50 | ppm |
| $t_j$ | RMS Period Jitter | | | | 1 | ps |
| $t_L$ | Clock Low Time | | 8 | | 12 | ns |
| $t_H$ | Clock High Time | | 8 | | 12 | ns |
| $t_R$ / $t_F$ | Clock Rise / Fall Time | 6pF load | | 2 | | ns |
| DC | Duty Cycle | | 45 | | 55 | % |

*Table 3.14* **50MHz Reference Clock Output Timing**

## 3.13 JTAG

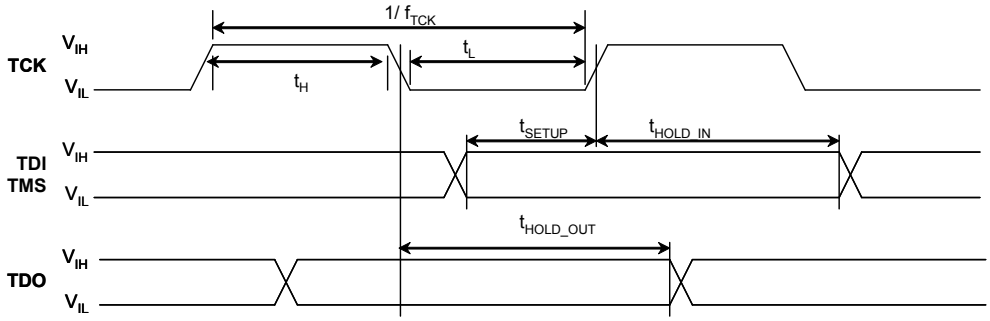


*Figure 3.14* **JTAG Timing Diagram**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{TCK}$ | Clock Frequency | | | | 20 | MHz |
| $t_L$ | Clock Low Time | | 20 | | | ns |
| $t_H$ | Clock High Time | | 20 | | | ns |
| $t_{SETUP}$ | Input Setup Time | | 10 | | | ns |
| $t_{HOLD\_IN}$ | Input Hold Time | | 15 | | | ns |
| $t_{HOLD\_OUT}$ | Output Hold Time | | 4 | | 22 | ns |

*Table 3.15* **JTAG Timing**

# Electrical Specifications 4

## 4.1 Absolute Maximum Ratings

| Symbol | Parameter | Test Condition | Min | Max | Units |
|---|---|---|---|---|---|
| VDD | 0.85V Digital Supply | | -0.5 | 0.935 | V |
| VA12 | 1.2V Analog Supply | | -0.5 | 1.32 | V |
| VA21 | 2.1V Analog Supply | | -0.5 | 2.31 | V |
| VDD_IO | 1.8V VDD General I/O Supply | | -0.5 | 1.98 | V |
| | 3.3V VDD General I/O Supply | | -0.5 | 3.63 | V |
| $T_{STORE}$ | Storage Temperature | | -50 | 150 | °C |

*Table 4.1* **AQR107-AQR109 Absolute Maximum Ratings**

## 4.2 Recommended Operating Conditions

| Symbol | Parameter | Test Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction Temperature | Extended Grade | 0 | 108 | °C |
| | | Industrial Grade | -40 | 108 | °C |
| $T_{JST}$ | Short-Term Junction Temperature[1] | | -- | 110 | °C |

*Table 4.2* **AQR107-AQR109 Recommended Operating Conditions**

1. In order to not degrade the life of the part, the AQR107-AQR109 should *not* be operated at this temperature for more than 1 week / year.

## 4.3 Power

The AQR107-AQR109 automatically adjusts is power consumption based on the length of the channel; consequently, there is no explicit “short-reach mode”†. However, the power consumption of the AQR107-AQR109 can be characterized over the IEEE 30-meter short-reach channel.

† Thus, when PHY power consumption is characterized at 30 meters, this is simply what represents the power consumption of the PHY when it is operating on a 30-meter link.

The following tables specify the power supply requirements and the operating current/power for the port for the AQR107-AQR109 in both full-reach and short-reach operation modes.

### 4.3.1 Operating Modes

The AQR107-AQR109 has several different operating regimes that each use different amounts of power. These regimes are listed as follows:

1) **Low power (LP)**: In this mode, everything is shut off except for the internal microprocessor and the MDIO interface, It is designed for out-of-service ports, and is the lowest power operating mode.

2) **Autonegotiation (ANEG)**: In this mode, the AQR107-AQR109 attempts to autonegotiate with the far-end PHY, and is sending and trying to receive link pulses. This is second lowest power operating mode, and usually lasts between 1.6 and 1.8 seconds†.

3) **Training (TRNG)**: This is the highest power mode, and occurs at the beginning of a 10GBASE-T/ 5GBASE-T/2.5GBASE-T/1000BASE-T link training session. This training mode lasts for a maximum of 2 seconds. This sets the maximum requirements for the VA12, VA21, and VDD power supplies.

4) **10G Steady-State Operation (10GSS)**: This is the second highest power mode, and occurs during normal steady-state link operations. This sets the maximum requirements for the thermal design, and is the maximum for the VDD power supply.

5) **5G Steady-State Operation (5GSS)**: This is the power mode seen during normal 5GBASE-T operations.

6) **2.5G Steady-State Operation (2.5GSS)**: This is the power mode seen during normal 2.5GBASE-T operations.

7) **1G Steady-State Operation (1GSS)**: This is the power mode seen during normal 1000BASE-T operations.

8) **100M Steady-State Operation (100MSS)**: This is the power mode seen during normal 100BASE-TX operations.

† This autonegotiation time assumes that an active link-partner is present. If one is not present, the AQR107-AQR109 continues attempting to autonegotiate until a PHY connection is made.

An example of the power consumption versus time for some of these modes in 10G operation is shown in Figure 4.1.

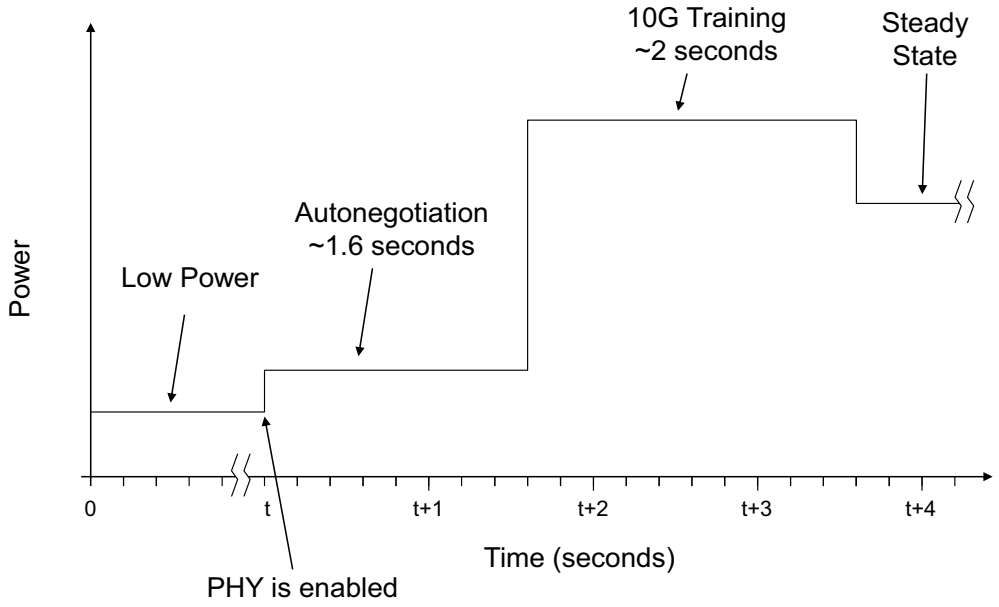


*Figure 4.1* **Power Versus Time**

In Figure 4.1, the device starts off in low-power mode, and then at time *t*, the AQR107-AQR109 is enabled, and autonegotiation begins. After 10GBASE-T is agreed on as the connection rate, 10GBASE-T training starts, and then after 2 seconds, it enters into the 10GBASE-T steady-state.

## 4.4 Power Supplies

### 4.4.1 VA21, VA12, and VDD Supply Specifications

Table 4.3 provides the DC and AC power supply requirements for the AQR107-AQR109:

- VA21 includes the following supplies: VA21 and VA21_XTAL.
- VA12 includes the following supplies: VA12 and V12_SRDS.
- VDD includes the following supplies: VDD and VDD_SRDS.

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $VA21_{TOTAL}$ | Input Voltage[1] | | 2.037 | 2.10 | 2.163 | V |
| $VA21_{RIPPLE}$ | Input Voltage Ripple | Peak to Peak | 0 | | 13 | mV |
| $VA12_{TOTAL}$ | Input Voltage[1] | | 1.164 | 1.20 | 1.236 | V |
| $VA12_{RIPPLE}$ | Input Voltage Ripple | Peak to Peak | 0 | | 48 | mV |
| $V_{VDDTOTAL}$ | Input Voltage[1] | | 0.8245 | 0.850 | 0.8755 | V |
| $V_{VDDRIPPLE}$ | Input Voltage Ripple | Peak to Peak | 0 | | 34 | mV |

*Table 4.3* **VA21, VA12, and VDD Electrical Parameters**

1. The input voltage is specified as DC accuracy.

## 4.5 Other Power Supplies

### 4.5.1 VDD_IO Supply Specifications

Table 4.4 provides DC and AC power supply requirements for the VDD_IO supply for the AQR107-AQR109. VDD_IO operates at either 1.8V or 3.3V.

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $VDD\_IO_{TOTAL}$ | 1.8V Input Voltage[1, 2] | | 1.75 | 1.8 | 1.85 | V |
| | 3.3V Input Voltage[1, 2] | | 3.20 | 3.30 | 3.40 | V |
| $VDD\_IO_{RIPPLE}$ | 1.8V Input Voltage Ripple | Peak to Peak | | | 72 | mV |
| | 3.3V Input Voltage Ripple | Peak to Peak | | | 132 | mV |

*Table 4.4* **VDD_IO Electrical Parameters**

1. The input voltage is specified as DC accuracy.
2. VDD_IO current varies with the MDIO load/activity and non-management I/O usage. Aquantia Corp. has reserved 100mA per port on the reference test boards as a worst-case condition.

## 4.6 Steady-State Operating Conditions

### 4.6.1 Typical Steady-State Operating Conditions

Table 4.5 provides the typical port steady-state current and power for the AQR107-AQR109.

| Symbol | Parameter | Test Condition | AQR107 (10G[1]) | AQR108 (5G[2]) | AQR109 (2.5G[2]) | Units |
|---|---|---|---|---|---|---|
| $I_{VA21TOTAL}$ | Input Current | Steady-State (typical) | 340 | 230 | 245 | mA |
| $I_{VA12TOTAL}$ | Input Current | Steady-State (typical) | 510 | 470 | 470 | mA |
| $I_{VDDTOTAL}$ | Input Current | Steady-State (typical) | 1570 | 1450 | 930 | mA |
| $P_{TOTAL\_TYP\_SS}$ | Power | Steady-State (typical) | 2.66 | 2.28 | 1.87 | W |

*Table 4.5* **Typical Steady-State Parameters**

1. Typical supplies, 30 meters Cat 6A, $T_J = 70^oC$.
2. Typical supplies, 30 meters Cat 5e, $T_J = 70^oC$.

### 4.6.2 Maximum Steady-State Operating Conditions

Table 4.6 provides the maximum port steady-state current and power for the AQR107-AQR109.

| Symbol | Parameter | Test Condition | AQR107 (10G[1]) | AQR108 (5G[2]) | AQR109 (2.5G[2]) | Units |
|---|---|---|---|---|---|---|
| $I_{VA21TOTAL}$ | Input Current | Steady-State (maximum) | 435 | 290 | 275 | mA |
| $I_{VA12TOTAL}$ | Input Current | Steady-State (maximum) | 610 | 560 | 560 | mA |
| $I_{VDDTOTAL}$ | Input Current | Steady-State (maximum) | 3100 | 2210 | 1530 | mA |
| $P_{TOTAL\_MAX\_SS}$ | Power | Steady-State (maximum) | 4.41 | 3.25 | 2.63 | W |

*Table 4.6* **Maximum Steady-State Parameters**

1. Maximum supplies, 100 meters Cat 6A, $T_J = 108^oC$.
2. Maximum supplies, 100 meters Cat 5e, $T_J = 108^oC$.

## 4.7 Instantaneous Current Consumption

Table 4.7 provides the maximum port transient current for the AQR107-AQR109. These values do not necessarily take place simultaneously and are intended to be used for voltage regulator (VR) design.

**Note:** The listed values are not representative of the device under steady-state operation.

| Symbol | Parameter | Test Condition | AQR107 (10G[1]) | AQR108 (5G[2]) | AQR109 (2.5G[2]) | Units |
|---|---|---|---|---|---|---|
| $I_{VA21TOTAL\_MAX}$ | Input Current for port | Training (maximum) | 435 | 290 | 275 | mA |
| $I_{VA12TOTAL\_MAX}$ | Input Current for port | Training (maximum) | 610 | 560 | 560 | mA |
| $I_{VDDTOTAL\_MAX}$ | Input Current for port | Training (maximum) | 3830 | 2640 | 1805 | mA |

*Table 4.7* **Training Parameters**

1. 10G Training, $T_J$ = 108°C.
2. 5G/2.5G Training, $T_J$ = 108°C.

## 4.8 Management Interface

The management interface includes the following signals:

*1)* MDC

*2)* MDIO

*3)* RST_N

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | | | | 0.54 | V |
| $V_{IH}$ | Input high voltage | | 1.26 | | | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = -4mA | 0.0 | | 0.2 | V |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = 0mA | | | | V |
| | | $I_{OH}$ = 10mA | | | | V |
| $I_{OL}$ | Output low current | $V_{OL}$ = 0.2V | | | | mA |
| $I_{OH}$[1] | Output high current | $V_{OH}$ = 1.0V | | | | mA |
| $I_{LKG}$ | Tristate Leakage | $V_{IN}$ = 0V or $V_{CC}$ | -10 | | 10 | µA |
| $C_i$ | Input capacitance | | | | 10 | pF |
| $C_L$ | Maximum capacitive load | | | | 470 | pF |

*Table 4.8* **1.8V Mode MDIO Electrical Interface Characteristics**

1. $I_{OH}$ parameter is not applicable to open drain drivers (for example, the MDIO data line).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage | | | | 30 | %VDD_IO |
| $V_{IH}$ | Input high voltage | | 70 | | | %VDD_IO |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = -4mA | 0 | | 20 | %VDD_IO |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = 0mA | 80 | | 120 | %VDD_IO |
| | | $I_{OH}$ = 10mA | 80 | | 120 | %VDD_IO |
| $I_{OL}$ | Output low current | $V_{OL}$ = 20% VDD_IO | 4 | | | mA |
| $I_{OH}$[1] | Output high current | $V_{OH}$ = 80% VDD_IO | | | 0 | mA |

*Table 4.9* **70% / 30% VDD_IO Mode MDIO Electrical Interface Characteristics**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LKG}$ | Tristate Leakage | $V_{IN}$ = 0V or $V_{CC}$ | -10 | | 10 | µA |
| $C_i$ | Input capacitance | | | | 10 | pF |
| $C_L$ | Maximum capacitive load | | | | 120 | pF |

*Table 4.9* **70% / 30% VDD_IO Mode MDIO Electrical Interface Characteristics** (continued)

1. $I_{OH}$ parameter is not applicable to open drain drivers (for example, the MDIO data line).

## 4.9 I/O

All of the non-management interface I/O on the AQR107-AQR109 run from VDD_IO and use the same I/O cell that has the following characteristics listed in Table 4.12.

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | | 30 | %VDD_IO |
| $V_{IH}$ | Input High Voltage | | 70 | | | %VDD_IO |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = -4mA | 0 | | 20 | %VDD_IO |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = 0mA | 80 | | 120 | %VDD_IO |
| | | $I_{OH}$ = 10mA | 80 | | 120 | %VDD_IO |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 20% VDD_IO | 17.79 | 30.17 | 42.71 | mA |
| $I_{OH}$[1] | Output High current | $V_{OH}$ = 80% VDD_IO | 16.67 | 26.33 | 39.32 | mA |
| $I_{LKG}$ | Tristate Leakage | $V_{IN}$ = 0V or $V_{CC}$ | -10 | | 10 | µA |
| $C_I$ | Input Capacitance | | | | 10 | pF |
| $C_L$ | Maximum Capacitive Load | | | | 120 | pF |

*Table 4.10* **I/O Pin Electrical Parameters**

1. $I_{OH}$ parameter is not applicable to open drain drivers (for example, the MDIO data line).

**Note:** The SPI interface is 3.3V tolerant.

## 4.10 Serial FLASH

Table 4.11 lists the SPI pin capacitance, and Table 4.12 lists the SPI DC characteristics.

| Symbol | Parameter | Test Condition | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ | Output Capacitance (SCLK, CS*, SOUT) | $V_{OUT}$ = 0V | 5 | pF |
| $C_{IN}$ | Input Capacitance (SIN) | $V_{IN}$ = 0V | 5 | pF |

*Table 4.11* **SPI Pin Capacitance**

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LKG}$ | Tristate Leakage | $V_{IN}$ = 0V or $V_{CC}$ | -10 | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | | | | 20 | %VDD_IO |
| $V_{IH}$ | Input High Voltage | | 80 | | | %VDD_IO |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4mA | | | 20 | %VDD_IO |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -4mA | 80 | | | %VDD_IO |
| $I_{OL}$ | Output low current | | 4 | | | mA |
| $I_{OH}$ | Output high current | | | | -4 | mA |

*Table 4.12* **SPI DC Characteristics**

## 4.11 SerDes

| Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Voltage[1] | Peak-to-peak differential | 400 | | 1000 | mV |
| Transmit Common Mode Voltage | | 200 | | 700 | mV |
| Differential Output Impedance | Programmable | 80 | 100 | 120 | Ω |
| Common Mode Output Impedance | | 20 | 25 | 30 | Ω |

*Table 4.13* **SerDes Transmitter Characteristics**

1. Near-end programmable output range.

| Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Voltage | Peak-to-peak differential | 50 | | 2000 | mV |
| Input Common Mode Voltage | Peak-to-peak differential | 650 | | 1000 | mV |
| Input Loss of Signal Voltage | Peak-to-peak differential | 75 | 120 | 175 | mV |
| Differential Input Impedance[1] | Programmable | 80 | | 120 | Ω |
| Common Mode Input Impedance | | 20 | 25 | 27.5 | Ω |
| Receiver Differential Return Loss | DC | -20 | | | dB |
| | 5GHz | -5 | | | dB |
| Receiver Common-Mode Return Loss | DC | -10 | | | dB |
| | 5GHz | -6 | | | dB |

*Table 4.14* **SerDes Receiver Characteristics**

1. This is programmable to ±10%.

## 4.12 Line (MDI)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{OH-DIFF}$ | Differential Output Voltage | | | | 2.0 | $V_{pk-pk}$ |
| $C_{IN}$ | Input Capacitance | | | | 2.5 | pF |
| $R_{IN}$ | Input Resistance | | 48 | 50 | 52 | Ω |

*Table 4.15* **MDI Electrical Parameters**

The AQR107-AQR109 uses a voltage-mode driver to drive the MDI, so only decoupling is required on the transformer center-tap.

## 4.13 Reference Clocks

### 4.13.1 Input Clock Pins XTAL_I and XTAL_O

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{SWING}$ | Single-Ended Input Voltage Swing | | 0.35 | | V |
| $V_{COMMON}$ | Common-Mode Voltage Level | | 1.2 | | V |
| $V_{IH}$ | Input High | | 1.375 | | V |
| $V_{IL}$ | Input Low | | 1.025 | | V |
| $C_{IN}$ | Input Capacitance | | | 1 | pF |
| $Z_{IN-DIFF}$ | Input Impedance | | 100 | | Ω |
| $R_{IN-DIFF}$ | Input Termination | | 100 | | Ω |

*Table 4.16* **LVDS 50MHz Input Electrical Parameters**

### 4.13.2 Input Clock Pins CLK_1588_P and CLK_1588_N

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{SWING}$ | Single-Ended Input Voltage Swing | | -0.175 | | V |
| $V_{COMMON}$ | Common-Mode Voltage Level[1] | | 0.175 | | V |
| $V_{IH}$ | Input High | 1.35 | 1.45 | 1.1025 | V |
| $V_{IL}$ | Input Low | 0.55 | 0.65 | 0.75 | V |
| $f_{CLK\_1588}$ | Operating Frequency | 40 | | 100 | MHz |
| $C_{IN}$ | Input Capacitance | | | 1 | pF |
| $Z_{IN-DIFF}$ | Input Impedance | | 100 | | Ω |
| $R_{IN-DIFF}$ | Input Termination | | 100 | | Ω |

*Table 4.17* **CLK_1588 Input Electrical Parameters**

1. CLK_1588 support AC-coupled LVDS and LVPECL clock.

## 4.14 Reference Resistors

| Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Reference Resistance | Tied to 0V | | 2.00 | | kΩ |
| Resistor Accuracy | | | | 1 | % |
| Maximum Power | | | | 5 | mW |
| Temperature Variation | | | 50 | | ppm/°C |

*Table 4.18* **Bandgap Reference Resistor Electrical Parameters**

# Package 5

## 5.1 Mechanical

The AQR107-AQR109 is packaged in a 7 mm x 11 mm flip-chip 104-pin exposed-die overmolded FCCSP (8 rows x 13 rows). Figure 5.1 and Figure 5.2 show the mechanical drawings of this package.

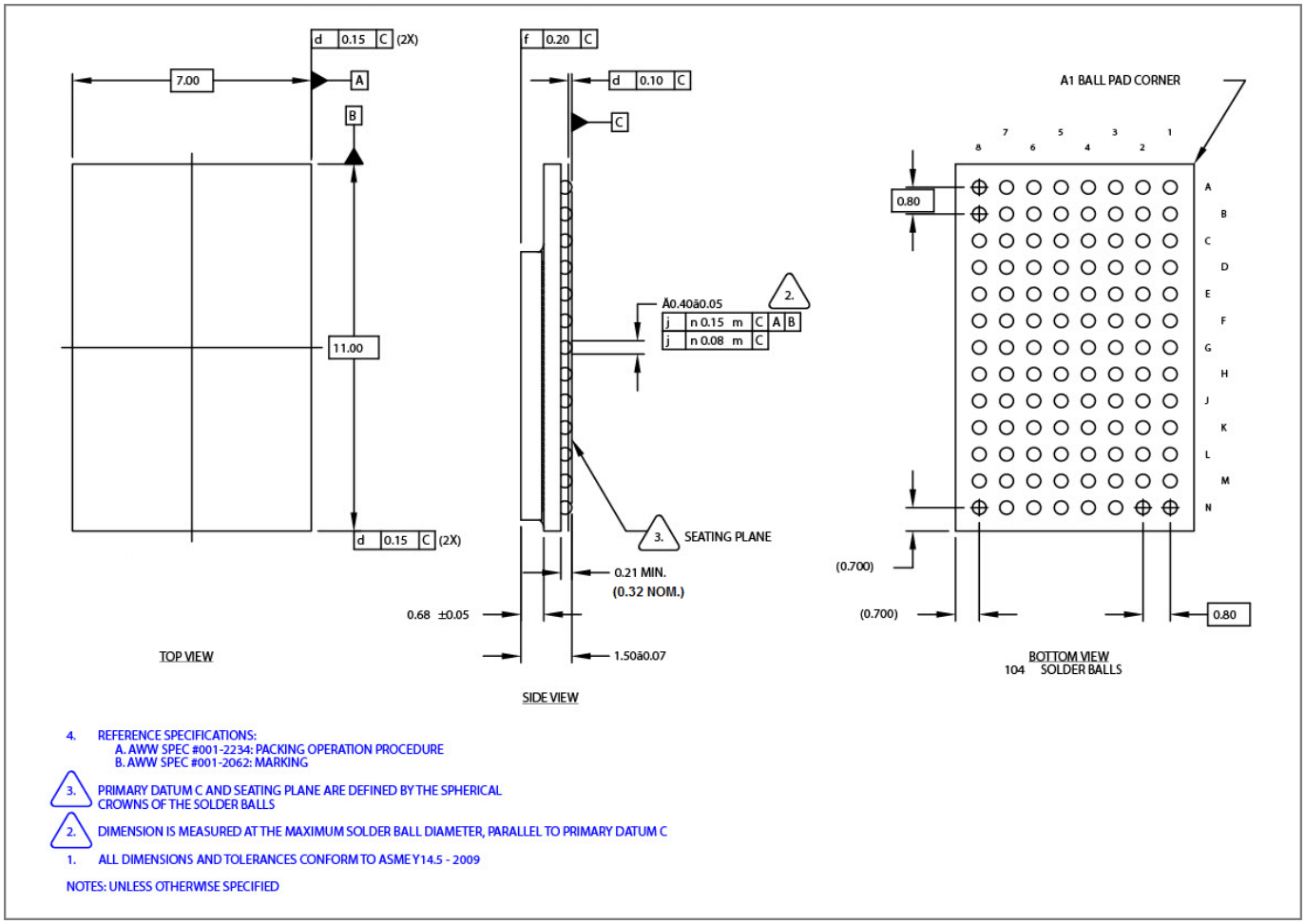


*Figure 5.1* **AQR107-AQR109 Mechanical Drawing 1**

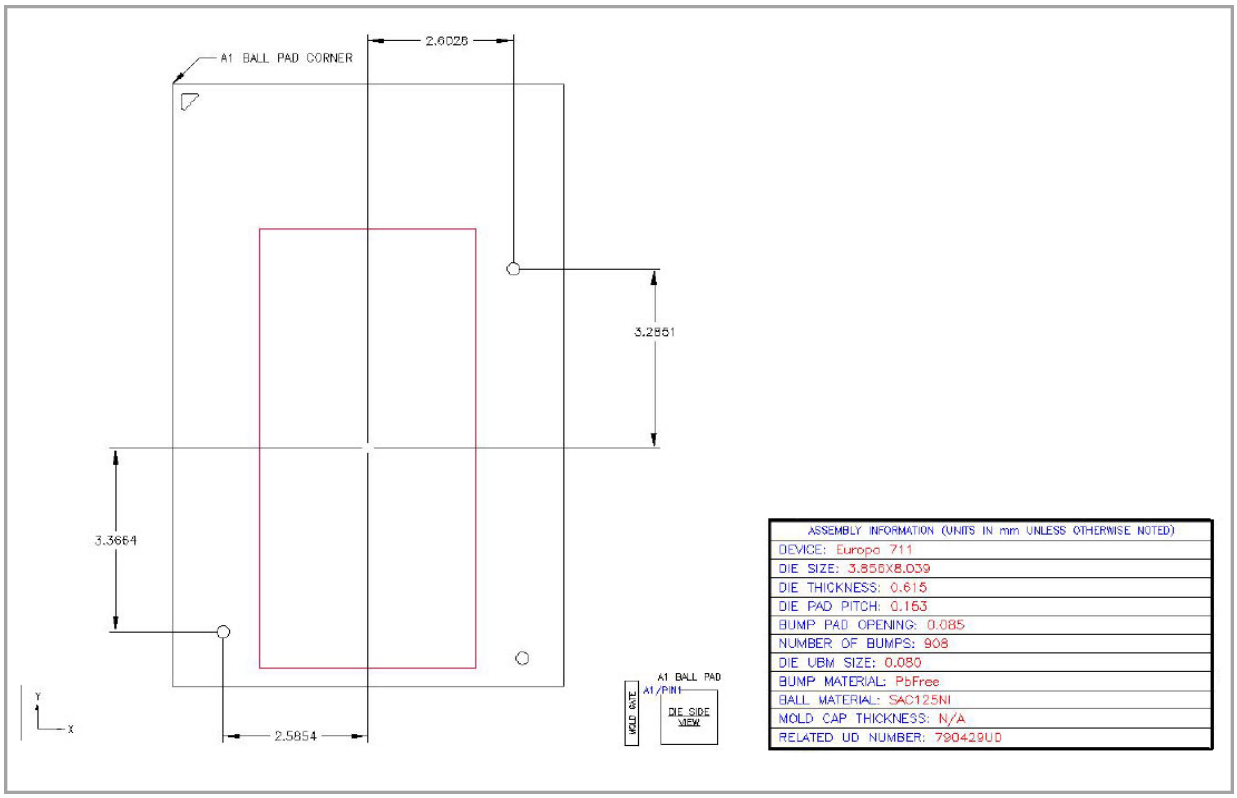


*Figure 5.2* **AQR107-AQR109 Mechanical Drawing 2**

## 5.2 Thermal

### 5.2.1 Theta Js

The values of the various $\theta_J$s are listed in Table 5.1:

| Name | Thermal Coefficient | Test Condition | Value | Units |
|---|---|---|---|---|
| Theta Junction to Ambient | $\theta_{JA}$ | Still air at 25°C | 19.58 | °C/W |
| Theta Junction to Board | $\theta_{JB}$ | JEDEC 2s2p[1] | 15.76 | °C/W |

*Table 5.1* **Theta J's**

1. Top/bottom trace 2 oz. copper.
   Middle planes 1 oz. copper.
   Equivalent 20% 2 oz. copper coverage adjacent to package.
   Bottom copper 2 oz. 20% coverage.

### 5.2.2 Thermal Model

For the AQR107-AQR109, Aquantia supplies a Flotherm® model with Packet Details Markup Language (PDML).

# Register Map 6

## 6.1 Introduction

The AQR107-AQR109 is internally divided into a series of MDIO Manageable Devices (MMDs), each of which performs a logical function as per the 10GBASE-T standard (Figure 6.1 shows a block diagram of this partitioning). Here the MMD #1 contains the PMA, which is basically the analog front-end of the chip. This is connected to MMD #3, which contains the PCS, which handles the 10GBASE-T transmission frame coding and decoding, including the 128-DSQ and LDPC work.

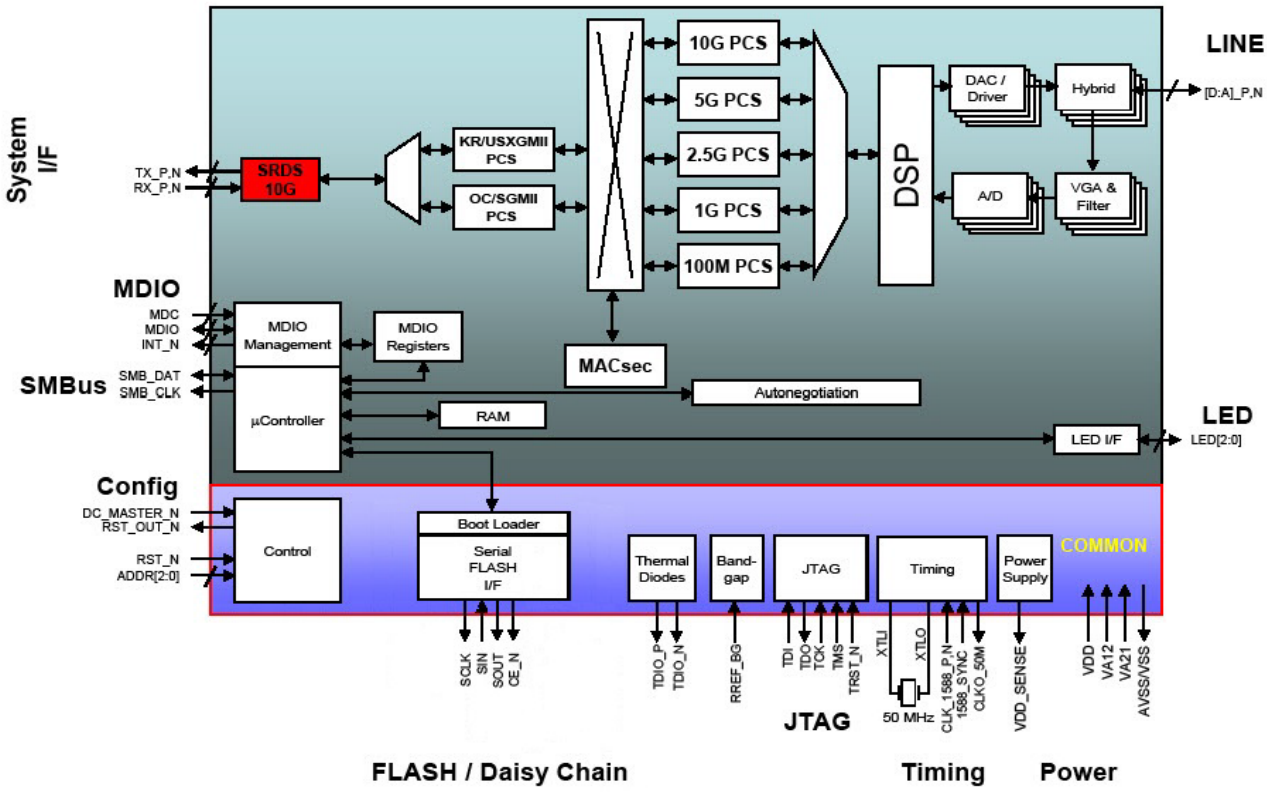


*Figure 6.1* **MDIO Manageable Devices Block Diagram**

This block is in turn connected to MMD #4, which contains the SerDes PCS. In addition to these MMDs, there are three others of note: MMD #7, which contains the autonegotiation function, MMD #29, which contains the controls for the GbE and 100M PCS machinery, and MMD# 30, which contains the global control functionality for the AQR107-AQR109.

Not shown, but present within the AQR107-AQR109, is another MMD, #31, which is used for proprietary purposes as an adjunct to the PMA.

## 6.2 Register Structure

Table 6.1 shows a map of these regions. Any attempt to read from the reserved MMD addresses will return a value of 0x00, and any writes to these addresses will have no effect.i

| 5-Bit Device Address (Hex) | MMD Name |
|---|---|
| 0 | reserved |
| 1 | PMA/PMD (128 DSQ) |
| 2 | reserved |
| 3 | PCS (64/65B coder/decoder) |
| 4 | PHY XS |
| 5 → 6 | reserved |
| 7 | Auto-negotiation |
| 8 → 1C | reserved |
| 1D | Clause 22 Extension |
| 1E | Global |
| 1F | Aquantia Proprietary |

*Table 6.1* **MMD Device Addresses**

## 6.3 Format and Nomenclature

Registers within the device are referenced in the following format:

**Region.Register.Bit**

Where ***Region*** corresponds to the MMD region that is being addressed, and ***Register*** corresponds to the register within that MMD region, and ***Bit*** corresponds to the bit within the specific register. All registers within the MDIO register space are 16 bits. The address of the register is the 16-bit MDIO address.

All read and write operation are *word based*, which means that the entire 16-bit register is read or written (versus individual bits being read or write). Within the MDIO register space, there are several different bit types. A list of these bit types is found in Table 6.2.

| Abbreviation | Type | Description |
|---|---|---|
| LL | Latching Low | If the condition the bit is monitoring goes low, this bit latches low, generates a maskable interrupt, and stays low until read. Reading this bit resets it to one. This bit is read-only. |
| LH | Latching High | If the condition the bit is monitoring goes high, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only. |
| LRF | Latch Rising or Falling | Set high on either a rising or falling edge. If a transition occurs, this bit latches high, generates a maskable interrupt, and stays high until read. Reading this bit resets it to zero. This bit is read-only. |
| PD | Provisionable Defaults | Indicates that the default value associated with this field is provisionable. |
| RO | Read Only | Read-only field. Writes are ignored. |
| ROS | Read Only Static | Read-only and static field. The value does not change. |
| R/W | Read / Write | Field can be both read from and written to. |
| SC | Self-Clearing | A read/write register which resets itself upon completion of an action. |
| SCT | Saturating Counter | A read-only counter that saturates at the limit, and is cleared on read. |
| SCTL | Saturating Counter LSW | The Least Significant Word of a Saturating Counter. This register clears the pair to zero on read and snapshots the mate MSW to shadow memory, awaiting read. |
| SCTM | Saturating Counter MSW | The Most Significant Word of a Saturating Counter. Reading this completes the read process of the register pair. |

*Table 6.2* **MDIO Register Space Bit Field Types**

## 6.4 Structure

The following structure is used for registers:

*1)* All Clause 45 registers (the registers that are defined in Clause 45) are placed in their respective areas within the MMDs as specified.

*2)* X2 registers are placed in MMD #1.

*3)* Aquantia-specific registers that are associated with each of the Clause 45 MMDs are placed in the Aquantia specific area beginning at 0xC000, according to the register map shown in Table 6.3.

| Base Offset (Hex) | Description |
|---|---|
| C000 | TX and Overall MMD Control |
| C400 | TX and Overall MMD Provisioning |
| C800 | TX and Overall MMD State |
| CC00 | TX and Overall MMD Alarms |
| D000 | Standard Interrupt Mask |
| D400 | TX and Overall MMD Interrupt Mask |
| D800 | TX and Overall MMD Debug |
| DC00 | Reserved |
| E000 | RX Control |
| E400 | RX Provisioning |
| E800 | RX State |
| EC00 | RX Alarms |
| F000 | Standard Interrupt Mask |
| F400 | RX Interrupt Mask |
| F800 | RX Debug |
| FC00 | Global Interrupt Flags |

*Table 6.3* **Register Layout**

The table is split into a transmit and a receive portion, with the transmit portion also containing any overall Aquantia specific registers for the MMD. Table 6.4 lists the following definitions that apply to the terms within the register layout.

| Term | Definition |
|---|---|
| Control | Action bits that affect the operation of the MMD, such as reset. |
| Provisioning | Static provisioning bits that control the behavior of the MMD. |
| State | Bits that reflect the state of the MMD. |

*Table 6.4* **Terms Used within the Register Layout**

| Term | Definition |
|---|---|
| Alarm | Bits that can generate maskable interrupts. |
| Standard Interrupt Mask | Interrupt masks for alarm bits defined in the Clause 45 register set. |
| Aquantia Specific Interrupt Mask | Interrupt masks for Aquantia Specific alarms. |

*Table 6.4* **Terms Used within the Register Layout** (continued)

*4)* Interrupts are handled in an hierarchical fashion, with the top level interrupt indication being the INT* interrupt pin on the AQR107-AQR109. Below this are two maskable interrupt trees: one tree is composed of standard interrupts, and the other tree is composed of Aquantia-defined interrupts.

The top level summary register for these trees resides at the end of the register space in MMD #30 - the Aquantia Global MMD (1E.FC00). Feeding this are interrupt registers from each of the individual MMDs.

*a)* The standard interrupt tree is designed so that the source of any interrupt can be determined in a maximum of two reads.

*b)* The Aquantia-defined interrupt tree requires at most three reads to determine the source of an interrupt.

*c)* All interrupts are maskable, whether they are from the Standard interrupt tree, or from the Aquantia-defined interrupt tree.

## 6.5 Registers and Documentation

The registers supporting the AQR107-AQR109 are described in the following sections of register tables, listed by the numerical order of their MMD address. Associated with these registers is a set of C-language header files and associated Doxygen documentation for them.

The header files contain all of the appropriate C-structures to access the registers and fields within the following sets of registers:


- “PMA Registers” on page 133
- “PCS Registers” on page 171
- “PHY XS Registers” on page 301
- “Autonegotiation Registers” on page 353

- “100BASE-TX and 1000BASE-T Registers” on page 421
- “Global Registers” on page 473

# 6.6 PMA Registers

### 6.6.1 PMA Standard Control 1: Address 1.0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Speed Selection LSB | {6,D}<br>1 1 = Speed set by Bits [5:2]<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s | R/W PD | 1 | |
| C | Reserved_0b | Reserved bit 12 | R/W PD | 0 | |
| B | Low Power | 1 = Low-power mode<br>0 = Normal operation | R/W PD | 0 | A one written to this register causes the PMA to enter low-power mode. If a global chip low-power state is desired, use Bit B in “Global Standard Control 1: Address 1E.0”.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| A:7 | Reserved_ 0c [A:7] | Reserved bits 10 to 7 | R/W PD | 0x0 | |
| 6 | Speed Selection MSB | {6,D}<br>1 1 = Speed set by Bits [5:2]<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s | R/W PD | 1 | |

*Table 6.6.1* **PMA Standard Control 1: Address 1.0**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5:2 | 10G Speed Selection [3:0] | 1 x x x = Reserved<br>0 1 1 1 = 5 Gb/s<br>0 1 1 0 = 2.5 Gb/s<br>0 1 0 1 = 400 Gb/s<br>0 1 0 0 = 25 Gb/s<br>0 0 1 1 = 100 Gb/s<br>0 0 1 0 = 40 Gb/s<br>0 0 0 1 = 10PASS-TS/2BASE-TL<br>0 0 0 0 = 10 Gb/s | R/W PD | 0x0 | |
| 1 | Reserved_0d | Reserved bit 1 | R/W PD | 0 | |
| 0 | Loopback | 1 = Enable loopback mode<br>0 = Normal operation | R/W PD | 0 | Enables the PMA Analog System Loopback.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F |

*Table 6.6.1* **PMA Standard Control 1: Address 1.0** (continued)

### 6.6.2 PMA Standard Status 1: Address 1.1

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved_ 1a [F:8] | Reserved bits 15 to 8 | R/W PD | 0x00 | |
| 7 | Fault | 1 = Fault condition detected<br>0 = No fault detected | RO | | Top-level fault indicator flag for the PMA. This bit is set if either of these two bits (1.8.B or 1.8.A) are set. |
| 6:3 | Reserved_ 1b [6:3] | Reserved bits 6 to 3 | R/W PD | 0x0 | |

*Table 6.6.2* **PMA Standard Status 1: Address 1.1**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | PMA Receive Link Status | Status of the PMA receive link<br>1 = Link up<br>0 = Link lost since last read | LL | | Indicates the status of the PMA receive link. This is the latch version of 1.E800.0. Note that this is latching low, so it can *only* be used to detect link drops, and not the current status of the link without performing back-to-back reads. |
| 1 | Low Power Ability | 1 = PMA supports low-power mode<br>0 = no low-power mode supported | ROS | 1 | Indicates whether the PHY supports a low-power mode. |
| 0 | Reserved_1c | Reserved bit 0 | R/W PD | 0 | |

*Table 6.6.2* **PMA Standard Status 1: Address 1.1** (continued)

### 6.6.3 PMA Standard Device Identifier 1: Address 1.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.6.3* **PMA Standard Device Identifier 1: Address 1.2**

### 6.6.4 PMA Standard Device Identifier 2: Address 1.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.6.4* **PMA Standard Device Identifier 2: Address 1.2**

### 6.6.5 PMA Standard Speed Ability: Address 1.4

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved_4a | Reserved bit 15 | ROS | 0 | |
| E | PMA 5G Capable | 1 = PMA is 5 Gb/s capable<br>0 = PMA is *not* 5 Gb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |
| D | PMA 2.5G Capable | 1 = PMA is 2.5 Gb/s capable<br>0 = PMA is *not* 2.5 Gb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |
| C:7 | Reserved_4b [C:7] | Reserved bits 12 to 7 | ROS | 0x00 | |
| 6 | PMA 10M Capable | 1 = PMA is 10 Mb/s capable<br>0 = PMA is *not* 10 Mb/s capable | ROS | 0 | Always set to 0 in the AQR107-AQR109. |
| 5 | PMA 100M Capable | 1 = PMA is 100 Mb/s capable<br>0 = PMA is *not* 100 Mb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |
| 4 | PMA 1G Capable | 1 = PMA is 1 Gb/s capable<br>0 = PMA is *not* 1 Gb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |
| 3 | Reserved_4c | Reserved bit 3 | ROS | 0 | |
| 2 | 10PASS-TS Capable | 1 = PMA is 10PASS-TS capable<br>0 = PMA is *not* 10PASS-TS capable | ROS | 0 | Always set to 0 in the AQR107-AQR109. |
| 1 | 2BASE-TL Capable | 1 = PMA is 2BASE-TL capable<br>0 = PMA is *not* 2BASE-TL capable | ROS | 0 | Always set to 0 in the AQR107-AQR109. |
| 0 | PMA 10G Capable | 1 = PMA is 10 Gb/s capable<br>0 = PMA is *not* 10 Gb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |

*Table 6.6.5* **PMA Standard Speed Ability: Address 1.4**

### 6.6.6 PMA Standard Devices in Package 1: Address 1.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as there is Autonegotiation in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no DTE XAUI interface in the AQR107-AQR109. |
| 4 | PHY XS Present | 1 = PHY XS is present in package<br>0 = PHY XS is *not* present in package | ROS | 1 | Always set to 1 as there is a PHY XS interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1 as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1 as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.6.6* **PMA Standard Devices in Package 1: Address 1.5**

### 6.6.7 PMA Standard Devices in Package 2: Address 1.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the Global registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the GbE registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.7* **PMA Standard Devices in Package 2: Address 1.6**

### 6.6.8 PMA Standard Control 2: Address 1.7

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved_7 [F:6] | Reserved bits 15 to 6 | R/W PD | 0x000 | |
| 5:0 | PMA Device Type [5:0] | [5:0]<br>5 4 3 2 1 0<br>1 1 0 0 0 1 = 5GBASE-T PMA/PMD type<br>1 1 0 0 0 0 = 2.5GBASE-T PMA/PMD type<br>0 0 1 1 1 1 = 10BASE-T PMA/PMD type<br>0 0 1 1 1 0 = 100BASE-TX PMA/PMD type<br>0 0 1 1 0 1 = 1000BASE-KX PMA/PMD type<br>0 0 1 1 0 0 = 1000BASE-T PMA/PMD type<br>0 0 1 0 1 1 = 10GBASE-KR PMA/PMD type<br>0 0 1 0 1 0 = 10GBASE-KX4 PMA/PMD type<br>0 0 1 0 0 1 = 10GBASE-T PMA type<br>0 0 1 0 0 0 = 10GBASE-LRM PMA/PMD type<br>0 0 0 1 1 1 = 10GBASE-SR PMA/PMD type<br>0 0 0 1 1 0 = 10GBASE-LR PMA/PMD type<br>0 0 0 1 0 1 = 10GBASE-ER PMA/PMD type<br>0 0 0 1 0 0 = 10GBASE-LX4 PMA/PMD type<br>0 0 0 0 1 1 = 10GBASE-SW PMA/PMD type<br>0 0 0 0 1 0 = 10GBASE-LW PMA/PMD type<br>0 0 0 0 0 1 = 10GBASE-EW PMA/PMD type<br>0 0 0 0 0 0 = 10GBASE-CX4 PMA/PMD type | R/W PD | 0x09 | Always set to 0x09 as the AQR107-AQR109 is a 10GBASE-T device. |

*Table 6.6.8* **PMA Standard Control 2: Address 1.7**

### 6.6.9 PMA Standard Status 2: Address 1.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 0x2, as the PMA is present in the AQR107-AQR109. |
| D | Transmit Fault Location Ability | 1 = PMA has the capability to detect a fault condition on the transmit path<br>0= PMA does *not* have the capability to detect a fault condition on the transmit path | ROS | 1 | Bit indicates whether the PMA has the ability to locate faults along the transmit path. |
| C | Receive Fault Location Ability | 1 = PMA has the capability to detect a fault condition on the receive path<br>0= PMA does *not* have the capability to detect a fault condition on the receive path | ROS | 1 | Bit indicates whether the PMA has the ability to locate faults along the receive path. |
| B | Transmit Fault | 1 = Fault condition on transmit path<br>0 = No fault condition on transmit path | LH | | Bit indicates whether there is a fault somewhere along the transmit path. This is a hardware fault and should never occur during normal operation. |
| A | Receive Fault | 1 = Fault condition on receive path<br>0 = No fault condition on receive path | LH | | Bit indicates whether there is a fault somewhere along the receive path.This is a hardware fault and should never occur during normal operation. |
| 9 | Extended Abilities | 1 = PMA has extended abilities listed in register 1.11<br>0= PMA does *not* have extended abilities | ROS | 1 | Field is set to 1, as the PMA in AQR107-AQR109 has extended abilities. |

*Table 6.6.9* **PMA Standard Status 2: Address 1.8**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 8 | PMD Transmit Disable Ability | 1 = PMD has the capability of disabling the transmitter<br>0= PMD does *not* have the capability of disabling the transmitter | ROS | 1 | Bit indicates whether the PMD has the capability of disabling its transmitter. Field is always set to 0x1, as the PMD in the AQR107-AQR109 has this ability. |
| 7 | PMA 10GBASE-SR Capable | 1 = PMA supports 10GBASE-SR<br>0 = PMA does *not* support 10GBASE-SR | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 6 | PMA 10GBASE-LR Capable | 1 = PMA supports 10GBASE-LR<br>0 = PMA does *not* support 10GBASE-LR | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 5 | PMA 10GBASE-ER Capable | 1 = PMA supports 10GBASE-ER<br>0 = PMA does *not* support 10GBASE-ER | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 4 | PMA 10GBASE-LX4 Capable | 1 = PMA supports 10GBASE-LX4<br>0 = PMA does *not* support 10GBASE-LX4 | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 3 | PMA 10GBASE-SW Capable | 1 = PMA supports 10GBASE-SW<br>0 = PMA does *not* support 10GBASE-SW | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 2 | PMA 10GBASE-LW Capable | 1 = PMA supports 10GBASE-LW<br>0 = PMA does *not* support 10GBASE-LW | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 1 | PMA 10GBASE-EW Capable | 1 = PMA supports 10GBASE-EW<br>0 = PMA does *not* support 10GBASE-EW | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 only supports 10GBASE-T. |
| 0 | PMA Loopback Ability | 1 = PMA supports loopback<br>0 = PMA does *not* support loopback | ROS | 1 | Always set to 1, as the PMA in the AQR107-AQR109 supports loopback. |

*Table 6.6.9* **PMA Standard Status 2: Address 1.8** (continued)

### 6.6.10 PMD Standard Transmit Disable Control: Address 1.9

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | PMD Channel 3 Transmit Disable | 1 = Disable output on transmit channel 3<br>0 = Normal operation | R/W PD | 0 | When disabled, the average launch power on a pair is set to less than -53 dBm.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| 3 | PMD Channel 2 Transmit Disable | 1 = Disable output on transmit channel 2<br>0 = Normal operation | R/W PD | 0 | |
| 2 | PMD Channel 1 Transmit Disable | 1 = Disable output on transmit channel 1<br>0 = Normal operation | R/W PD | 0 | |
| 1 | PMD Channel 0 Transmit Disable | 1 = Disable output on transmit channel 0<br>0 = Normal operation | R/W PD | 0 | |
| 0 | PMD Global Transmit Disable | 1 = Disable output on all channels<br>0 = Normal operation | R/W PD | 0 | When set, this bit disables (and overrides) all four channels, and sets the average launch power on all pairs to less than -53 dBm.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.6.10* **PMD Standard Transmit Disable Control: Address 1.9**

### 6.6.11 PMD Standard Signal Detect: Address 1.A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | PMD Channel 3 Signal Detect | 1 = Signal detected on receive channel 3<br>0 = No signal detected | RO | | Bits indicate the presence of signals on a given pair. A signal is defined as an autonegotiation pulse or Ethernet signals. |
| 3 | PMD Channel 2 Signal Detect | 1 = Signal detected on receive channel 2<br>0 = No signal detected | RO | | |
| 2 | PMD Channel 1 Signal Detect | 1 = Signal detected on receive channel 1<br>0 = No signal detected | RO | | |
| 1 | PMD Channel 0 Signal Detect | 1 = Signal detected on receive channel 0<br>0 = No signal detected | RO | | |
| 0 | PMD Global Signal Detect | 1 = Signals detected on all required channels<br>0 = No signal detected | RO | | Bit is marked when all required, valid Ethernet signals to create a connection are present on the line. |

*Table 6.6.11* **PMD Standard Signal Detect: Address 1.A**

### 6.6.12 PMD Standard 10G Extended Ability Register: Address 1.B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved_b0 | Reserved bit 15 | ROS | 0 | |
| E | PMA 2.5/5GBASE-T Capable | 1 = PMA capable of 2.5/5GBASE-T<br>0 = PMA incapable of 2.5/5GBASE-T | ROS | 1 | Field is set to 1, as the PMA in the AQR107-AQR109 supports 2.5/5GBASE-T. |
| D:9 | Reserved_b1 [D:9] | Reserved bits 13 to 9 | ROS | 0x00 | |
| 8 | PMA 10BASE-T Capable | 1 = PMA capable of 10BASE-T<br>0 = PMA incapable of 10BASE-T | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 does *not* support 10BASE-TX. |

*Table 6.6.12* **PMD Standard 10G Extended Ability Register: Address 1.B**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | PMA 100BASE-TX Capable | 1 = PMA capable of 100BASE-TX<br>0 = PMA incapable of 100BASE-TX | ROS | 1 | Field is always set to 1, as the PMA in the AQR107-AQR109 supports 100BASE-TX. |
| 6 | PMA 1000BASE-KX Capable | 1 = PMA capable of 1000BASE-KX<br>0 = PMA incapable of 1000BASE-KX | ROS | 1 | Field is always set to 1, as the PMA in the AQR107-AQR109 supports 1000BASE-KX. |
| 5 | PMA 1000BASE-T Capable | 1 = PMA capable of 1000BASE-T<br>0 = PMA incapable of 1000BASE-T | ROS | 1 | Field is set to 1, as the PMA in the AQR107-AQR109 supports 1000BASE-T. |
| 4 | PMA 10GBASE-KR Capable | 1 = PMA capable of 10GBASE-KR<br>0 = PMA incapable of 10GBASE-KR | ROS | 1 | Field is set to 1, as the PMA in the AQR107-AQR109 supports 10GBASE-KR. |
| 3 | PMA 10GBASE-KX4 Capable | 1 = PMA capable of 10GBASE-KX4<br>0 = PMA incapable of 10GBASE-KX4 | ROS | 1 | Field is set to 1, as the PMA in the AQR107-AQR109 supports 10GBASE-KX4. |
| 2 | PMA 10GBASE-T Capable | 1 = PMA capable of 10GBASE-T<br>0 = PMA incapable of 10GBASE-T | ROS | 1 | Field is set to 1, as the PMA in the AQR107-AQR109 supports 10GBASE-T. |
| 1 | PMA 10GBASE-LRM Capable | 1 = PMA capable of 10GBASE-LRM<br>0 = PMA incapable of 10GBASE-LRM | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 does *not* support 10GBASE-LRM. |
| 0 | PMA 10GBASE-CX4 Capable | 1 = PMA capable of 10GBASE-CX4<br>0 = PMA incapable of 10GBASE-CX4 | ROS | 0 | Field is always set to 0, as the PMA in the AQR107-AQR109 does *not* support 10GBASE-CX4. |

*Table 6.6.12* **PMD Standard 10G Extended Ability Register: Address 1.B** (continued)

### 6.6.13 PMA Standard Package Identifier 1: Address 1.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31-16 of Package ID | RO | | |

*Table 6.6.13* **PMA Standard Package Identifier 1: Address 1.E**

### 6.6.14 PMA Standard Package Identifier 2: Address 1.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15-0 of Package ID | RO | | |

*Table 6.6.14* **PMA Standard Package Identifier 2: Address 1.F**

### 6.6.15 PMA Reserved 14 Register: Address 1.14

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_14 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.6.15* **PMA Reserved 14 Register: Address 1.14**

### 6.6.16 PMA Extended Ability Register: Address 1.15

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved_15 [F:2] | Reserved bits [15:2] | ROS | 0x0000 | |
| 1 | 5GBASE-T Ability | 1 = PMA/PMD is able to perform 5GBASE-T<br>0 = PMA/PMD is *not* able to perform 5GBASE-T | ROS | 1 | |
| 0 | 2.5GBASE-T Ability | 1 = PMA/PMD is able to perform 2.5GBASE-T<br>0 = PMA/PMD is *not* able to perform 2.5GBASE-T | ROS | 1 | |

*Table 6.6.16* **PMA Extended Ability Register: Address 1.15**

### 6.6.17 PMA Reserved 16 Register: Address 1.16

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_16 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.6.17* **PMA Reserved 16 Register: Address 1.16**

### 6.6.18 PMA Reserved 17 Register: Address 1.17

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_17 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.6.18* **PMA Reserved 17 Register: Address 1.17**

### 6.6.19 PMA Reserved 18 Register: Address 1.18

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_18 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.6.19* **PMA Reserved 18 Register: Address 1.18**

### 6.6.20 PMA 10GBASE-T Status: Address 1.81

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Link Partner Information Valid | 1 = 10GBASE-T Link Partner information is valid<br>0 = 10GBASE-T Link Partner information is *not* valid | RO | | When set, this bit indicates that the startup protocol (55.4.2.5) has completed. |

*Table 6.6.20* **PMA 10GBASE-T Status: Address 1.81**

### 6.6.21 PMA 10GBASE-T Pair Swap and Polarity Status: Address 1.82

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B:8 | Pair Polarity [3:0] | 1 = Polarity of Pair is reversed<br>0 = Polarity of Pair is normal<br>[3] = Pair D Polarity<br>[2] = Pair C Polarity<br>[1] = Pair B Polarity<br>[0] = Pair A Polarity | RO | | When set, this bit indicates that the wires on the respective pair are reversed. |
| 7:2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | MDI / MD-X Connection State [1:0] | [1:0]<br>1 1 = No crossover<br>1 0 = Pair A/B crossover<br>0 1 = Pair C/D crossover<br>0 0 = Pair A/B and C/D crossover | RO | | These two bits indicate the current status of pair swaps at the MDI/MD-X. |

*Table 6.6.21* **PMA 10GBASE-T Pair Swap and Polarity Status: Address 1.82**

### 6.6.22 PMA 10GBASE-T TX Power Backoff and Short-Reach Setting: Address 1.83

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Link Partner TX Power Backoff [2:0] | [F:D]<br>0x7 = 14dB<br>0x6 = 12dB<br>0x5 = 10dB<br>0x4 = 8dB<br>0x3 = 6dB<br>0x2 = 4dB<br>0x1 = 2dB<br>0x0 = 0dB | RO | | The power backoff of the link partner. |
| C:A | TX Power Backoff [2:0] | [C:A]<br>0x7 = 14dB<br>0x6 = 12dB<br>0x5 = 10dB<br>0x4 = 8dB<br>0x3 = 6dB<br>0x2 = 4dB<br>0x1 = 2dB<br>0x0 = 0dB | RO | | The power backoff of the PMA. |
| 9:1 | Reserved_83 [9:1] | Reserved bits 9 to 1 | R/W PD | 0x000 | |
| 0 | Short-Reach Mode | 1 = Set PMA to operate in short-reach mode<br>0 = PMA is in normal operation | R/W PD | 0 | When set, this bit places the PMA into short-reach mode. |

*Table 6.6.22* **PMA 10GBASE-T TX Power Backoff and Short-Reach Setting: Address 1.83**

### 6.6.23 PMA 10GBASE-T Test Modes: Address 1.84

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Test Mode Control [2:0] | [F:D]<br>0x7 = Pseudo random test mode for BER Monitor<br>0x6 = Transmitter Droop test<br>0x5 = PSD and power level test<br>0x4 = Transmitter distortion test<br>0x3 = Slave mode jitter test<br>0x2 = Master mode jitter test<br>0x1 = Master source for slave mode jitter test<br>0x0 = Normal operation | R/W PD | 0x0 | Test mode control for the PMA as defined in Section 55.5.2 of 802.3an.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| C:A | Transmitter Test Frequencies [2:0] | [C:A]<br>0x7 = Reserved<br>0x6 = Dual Tone #5<br>0x5 = Dual Tone #4<br>0x4 = Dual Tone #3<br>0x3 = Reserved<br>0x2 = Dual Tone #2<br>0x1 = Dual Tone #1<br>0x0 = Reserved | R/W PD | 0x0 | The test frequencies associated with Test Mode #4 in [F:D]. |
| 9:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.23* **PMA 10GBASE-T Test Modes: Address 1.84**

### 6.6.24 PMA 10GBASE-T SNR Operating Margin Channel A: Address 1.85

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel A Operating Margin [F:0] | Operating margin (dB) of Channel A | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.24* **PMA 10GBASE-T SNR Operating Margin Channel A: Address 1.85**

### 6.6.25 PMA 10GBASE-T SNR Operating Margin Channel B: Address 1.86

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel B Operating Margin [F:0] | Operating margin (dB) of Channel B | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.25* **PMA 10GBASE-T SNR Operating Margin Channel B: Address 1.86**

### 6.6.26 PMA 10GBASE-T SNR Operating Margin Channel C: Address 1.87

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel C Operating Margin [F:0] | Operating margin (dB) of Channel C | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.26* **PMA 10GBASE-T SNR Operating Margin Channel C: Address 1.87**

### 6.6.27 PMA 10GBASE-T SNR Operating Margin Channel D: Address 1.88

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel D Operating Margin [F:0] | Operating margin (dB) of Channel D | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.27* **PMA 10GBASE-T SNR Operating Margin Channel D: Address 1.88**

### 6.6.28 PMA 10GBASE-T SNR Minimum Operating Margin Channel A: Address 1.89

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel A Minimum Operating Margin [F:0] | Minimum operating margin (dB) of Channel A since the last link up | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.32* **PMA 10GBASE-T SNR Minimum Operating Margin Channel A: Address 1.89**

### 6.6.29 PMA 10GBASE-T SNR Minimum Operating Margin Channel B: Address 1.8A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel B Minimum Operating Margin [F:0] | Minimum operating margin (dB) of Channel B since the last link up | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.29* **PMA 10GBASE-T SNR Minimum Operating Margin Channel B: Address 1.8A**

### 6.6.30 PMA 10GBASE-T SNR Minimum Operating Margin Channel C: Address 1.8B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel C Minimum Operating Margin [F:0] | Minimum operating margin (dB) of Channel C since the last link up | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.30* **PMA 10GBASE-T SNR Minimum Operating Margin Channel C: Address 1.8B**

### 6.6.31 PMA 10GBASE-T SNR Minimum Operating Margin Channel D: Address 1.8C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel D Minimum Operating Margin [F:0] | Minimum operating margin (dB) of Channel D since the last link up | RO | | The excess SNR that is enjoyed by the channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.6.31* **PMA 10GBASE-T SNR Minimum Operating Margin Channel C: Address 1.8C**

### 6.6.32 PMA 10GBASE-T Receive Signal Power Channel A: Address 1.8D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel A Received Signal Power [F:0] | Received signal power (dBm) for Channel A | RO | | The received signal power on the channel. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -20.0dB to +5.5dB. The number is in offset two's complement notation, with 0.0dB represented by 0x8000. |

*Table 6.6.32* **PMA 10GBASE-T Receive Signal Power Channel A: Address 1.8D**

### 6.6.33 PMA 10GBASE-T Receive Signal Power Channel B: Address 1.8E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel B Received Signal Power [F:0] | Received signal power (dBm) for Channel B | RO | | The received signal power on the channel. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -20.0dB to +5.5dB. The number is in offset two's complement notation, with 0.0dB represented by 0x8000. |

*Table 6.6.33* **PMA 10GBASE-T Receive Signal Power Channel B: Address 1.8E**

### 6.6.34 PMA 10GBASE-T Receive Signal Power Channel C: Address 1.8F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel C Received Signal Power [F:0] | Received signal power (dBm) for Channel C | RO | | The received signal power on the channel. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -20.0dB to +5.5dB. The number is in offset two's complement notation, with 0.0dB represented by 0x8000. |

*Table 6.6.34* **PMA 10GBASE-T Receive Signal Power Channel C: Address 1.8F**

### 6.6.35 PMA 10GBASE-T Receive Signal Power Channel D: Address 1.90

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel D Received Signal Power [F:0] | Received signal power (dBm) for Channel D | RO | | The received signal power on the channel. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -20.0dB to +5.5dB. The number is in offset two's complement notation, with 0.0dB represented by 0x8000. |

*Table 6.6.35* **PMA 10GBASE-T Receive Signal Power Channel D: Address 1.90**

### 6.6.36 PMA 10GBASE-T Skew Delay 1: Address 1.91

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:8 | Skew Delay B [6:0] | Skew delay for pair B | RO | | The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25ns resolution to an accuracy of 2.5ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-80ns to +78.75ns), the field displays the maximum respective value. |
| 7:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.36* **PMA 10GBASE-T Skew Delay 1: Address 1.91**

### 6.6.37 PMA 10GBASE-T Skew Delay 2: Address 1.92

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:8 | Skew Delay D [6:0] | Skew delay for pair D | RO | | The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25ns resolution to an accuracy of 2.5ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-80ns to +78.75ns), the field displays the maximum respective value. |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | Skew Delay C [6:0] | Skew delay for pair C | RO | | The skew delay reports the current skew delay on each of the pair with respect to physical pair A. It is reported with 1.25ns resolution to an accuracy of 2.5ns. The number is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-80ns to +78.75ns), the field displays the maximum respective value. |

*Table 6.6.37* **PMA 10GBASE-T Skew Delay 2: Address 1.92**

### 6.6.38 PMA 10GBASE-T Fast Retrain Status and Control: Address 1.93

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | LP Fast Retrain Count [4:0] | Counts the number of fast retrains requested by the link partner | SCT | 0x00 | Saturating clear on read counter. |
| A:6 | LD Fast Retrain Count [4:0] | Counts the number of fast retrains requested by the local device | SCT | 0x00 | Saturating clear on read counter. |
| 5 | Reserved_93 | Reserved bit 5 | R/W PD | 0 | |
| 4 | Fast Retrain Ability | 1 = Fast retrain capability is supported<br>0 = Fast retrain capability is *not* supported | RO | | |
| 3 | Fast Retrain Negotiated | 1 = Fast retrain capability was negotiated<br>0 = Fast retrain capability was *not* negotiated | RO | | |
| 2:1 | Fast Retrain Signal Type [1:0] | 11 = Reserved<br>10 = PHY signals Link Interruption during fast retrain<br>01 = PHY signals Local Fault during fast retrain<br>00 = PHY signals IDLE during fast retrain | R/W | 0x0 | |
| 0 | Fast Retrain Enable | 1 = Fast retrain capability is enabled<br>0 = Fast retrain capability is disabled | R/W | 0 | |

*Table 6.6.38* **PMA 10GBASE-T Fast Retrain Status and Control: Address 1.93**

### 6.6.39 TimeSync PMA Capability: Address 1.708

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | TimeSync Transmit Path Data Delay | 1 = PMA provides information on transmit path data delay in registers 1.1801 through 1.1804<br>0 = PMA does *not* provide information on transmit path data delay | RO | | |
| 0 | TimeSync Receive Path Data Delay | 1 = PMA provides information on receive path data delay in registers 1.1805 through 1.1808<br>0 = PMA does *not* provide information on receive path data delay | RO | | |

*Table 6.6.39* **TimeSync PMA Capability: Address 1.708**

### 6.6.40 TimeSync PMA Transmit Path Data Delay 1: Address 1.709

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PMA Transmit Path Data Delay LSW [F:0] | LSW of maximum PMA transmit delay in nanoseconds | RO | | |

*Table 6.6.40* **TimeSync PMA Transmit Path Data Delay 1: Address 1.709**

### 6.6.41 TimeSync PMA Transmit Path Data Delay 2: Address 1.70A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PMA Transmit Path Data Delay MSW [F:0] | Most Significant Word (MSW) of maximum PMA transmit delay in nanoseconds | RO | | |

*Table 6.6.41* **TimeSync PMA Transmit Path Data Delay 2: Address 1.70A**

### 6.6.42 TimeSync PMA Transmit Path Data Delay 3: Address 1.70B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PMA Transmit Path Data Delay LSW [F:0] | Least Significant Word (LSW) of minimum PMA transmit delay in nanoseconds | RO | | |

*Table 6.6.42* **TimeSync PMA Transmit Path Data Delay 3: Address 1.70B**

### 6.6.43 TimeSync PMA Transmit Path Data Delay 4: Address 1.70C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PMA Transmit Path Data Delay MSW [F:0] | MSW of minimum PMA transmit delay in nanoseconds | RO | | |

*Table 6.6.43* **TimeSync PMA Transmit Path Data Delay 4: Address 1.70C**

### 6.6.44 TimeSync PMA Receive Path Data Delay 1: Address 1.70D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PMA Receive Path Data Delay LSW [F:0] | LSW of maximum PMA receive delay in nanoseconds | RO | | |

*Table 6.6.44* **TimeSync PMA Receive Path Data Delay 1: Address 1.70D**

### 6.6.45 TimeSync PMA Receive Path Data Delay 2: Address 1.70E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PMA Receive Path Data Delay MSW [F:0] | MSW of maximum PMA receive delay in nanoseconds | RO | | |

*Table 6.6.45* **TimeSync PMA Receive Path Data Delay 2: Address 1.70E**

### 6.6.46 TimeSync PMA Receive Path Data Delay 3: Address 1.70F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PMA Receive Path Data Delay LSW [F:0] | LSW of minimum PMA receive delay in nanoseconds | RO | | |

*Table 6.6.46* **TimeSync PMA Receive Path Data Delay 3: Address 1.70F**

### 6.6.47 TimeSync PMA Receive Path Data Delay 4: Address 1.710

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PMA Receive Path Data Delay MSW [F:0] | MSW of minimum PMA receive delay in nanoseconds | RO | | |

*Table 6.6.47* **TimeSync PMA Receive Path Data Delay 4: Address 1.710**

### 6.6.48 PMA Transmit Reserved Vendor Provisioning: Address 1.C412

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Test Mode Rate [1:0] | 2 = 2.5G Test Modes<br>1 = 5G Test Modes<br>0 = 10G Test Mode | R/W PD | 0x0 | Field controls the data rate for the test mode activated with register 1.84. |
| D:4 | Reserved Spare Transmit Provisioning [9:0] | Reserved for future use | R/W PD | 0x000 | |
| 3:0 | Polarity Invert Enable [3:0] | 1 = Invert corresponding TX lane | R/W | 0x0 | Bit 0 corresponds to Lane A, Bit 1 to Lane B, and so on..., etc. |

*Table 6.6.48* **PMA Transmit Reserved Vendor Provisioning 0: Address 1.C412**

### 6.6.49 PMA Transmit Reserved Vendor Provisioning: Address 1.C413

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Channel Mask[3:0] | Channel mask specifying which channels will be affected by the TX PSD target | R/W PD | 0x0 | |
| B:8 | Reserved Spare Transmit Provisioning [3:0] | Reserved for future use | R/W PD | 0x0 | |
| 7:0 | Incremental TX PSD Target [7:0] | Deviation from the current TX PSD target based on registers A.A and A.B in 2's complement form s7 | R/W PD | 0x00 | |

*Table 6.6.49* **PMA Transmit Reserved Vendor Provisioning 1: Address 1.C413**

### 6.6.50 PMA Transmit Vendor Alarms 3: Address 1.CC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved PMA Transmit Alarms 3 [D:0] | Reserved for internal use | LH | | |
| 0 | Reset Complete | 1 = Hardware and Firmware reset has completed | LH | | This bit is a mirror of 1E.CC00.6, but has associated with it a known zero bit that can be used to ascertain that hardware reset has completed, enabling Reset Complete to be read in one shot without double polling and dealing with tristate MDIO issues. It avoids of problem of *not* knowing if/when the hardware complete phase of a reset has occurred when double-polling. |

*Table 6.6.50* **PMA Transmit Vendor Alarms 3: Address 1.CC02**

### 6.6.51 PMA Transmit Standard Interrupt Mask 1: Address 1.D000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PMA Receive Link Status Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Mask for Bit 1.1.2. |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.51* **PMA Transmit Standard Interrupt Mask 1: Address 1.D000**

### 6.6.52 PMA Transmit Standard Interrupt Mask 2: Address 1.D001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B | Transmit Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit 1.8.B |
| A | Receive Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit 1.8.A |
| 9:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.52* **PMA Transmit Standard Interrupt Mask 2: Address 1.D001**

### 6.6.53 PMA Transmit Vendor Interrupt Mask 3: Address 1.D402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 0 | Reset Complete Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.6.53* **PMA Transmit Vendor Interrupt Mask 3: Address 1.D402**

### 6.6.54 PMA Transmit Vendor Debug 1: Address 1.D800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PMA Digital System Loopback | 1 = Enables PMA digital system loopback | R/W PD | 0 | |
| E:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.6.54* **PMA Transmit Vendor Debug 1: Address 1.D800**

### 6.6.55 PMA Receive Reserved Vendor Provisioning 1: Address 1.E400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | External PHY Loopback | 1 = Enables external PHY loopback<br>0 = Normal operation | R/W PD | 0 | External PHY loopback expects a loopback connector such that Pair A is connected to Pair B, and Pair C is connected to Pair D.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| E:3 | Reserved Receive Provisioning 1 [B:0] | Reserved for future use | R/W PD | 0x000 | |
| 2 | Enable Aquantia Fast Retrain | 1 = Enables PMA Fast Link Retrain<br>0 = Disables PMA Fast Link Retrain | R/W PD | 0 | If the link partner is an Aquantia PHY and also has Fast Retrain enabled, use a special retrain sequence to bring the link back up without going back through the Autonegotiation sequence. |

*Table 6.6.55* **PMA Receive Reserved Vendor Provisioning 1: Address 1.E400**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | Force MDI Configuration | 1 = Ignore state of MDI_CFG pin<br>0 = Set MDI Configuration based on state of MDI_CFG | R/W PD | 0 | Normally, the MDI reversal configuration is taken from the MDI_CFG pin. If the Force MDI Configuration bit is asserted, the MDI_CFG pin is ignored and the current provisioned value of the MDI configuration bit is used instead. |
| 0 | MDI Configuration | 1 = MDI Reversed (ABCD -> DCBA)<br>0 = MDI Normal (ABCD -> ABCD) | R/W PD | 0 | Setting this bit determines if the MDI is reversed or not. Note that the reversal does not change pair polarity; for example, A+ maps to D+, etc.<br><br>The bit value is set during autonegotiation to the value of the MDI_CFG pin unless the Force MDI Configuration bit (1.E400.1) is asserted.<br><br>When the Force MDI Configuration bit is asserted, the MDI_CFG pin is ignored and this bit is unchanged from its default or provisioned value.<br><br>If this bit is changed manually after the autonegotiation completes, autonegotiation must be restarted to achieve the desired MDI configuration. |

*Table 6.6.55* **PMA Receive Reserved Vendor Provisioning 1: Address 1.E400** (continued)

### 6.6.56 PMA Receive Vendor State 1: Address 1.E800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PMA Receive Link Current Status | 1 = RX link is good | RO | | This is the current state of 1.1.2. |

*Table 6.6.56* **PMA Receive Vendor State 1: Address 1.E800**

### 6.6.57 PMA Receive Reserved Vendor State 1: Address 1.E810

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Accumulated Fast Retrain Time[F:0] | Accumulated time in milliseconds spent in fast retrain since the last auto-negotiation sequence | RO | | This is a saturating register. |

*Table 6.6.57* **PMA Receive Reserved Vendor State 1: Address 1.E810**

### 6.6.58 PMA Receive Reserved Vendor State 2: Address 1.E811

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Total Number Of Link Recovery Events Since Last AutoNeg [7:0] | The count of the cumulative number of Link Recovery Events since last autonegotiation | RO | | Register is automatically reset to 0 during Auto-negotiation. It increments once for each series of back-to-back Fast Retrain events. The result is reported modulo 256 (wrap around). |
| 7:0 | Total Number Of RFI Training Link Recovery Events Since Last AutoNeg [7:0] | The count of the cumulative number of RFI Training Link Recovery Events since last autonegotiation | RO | | This register is automatically reset to 0 during Autonegotiation. The result is reported modulo 256 (wrap around). |

*Table 6.6.58* **PMA Receive Reserved Vendor State 2: Address 1.E811**

### 6.6.59 PMA Vendor Global Interrupt Flags 1: Address 1.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific TX Alarms 1 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “PMA Transmit Vendor Alarms 1: Address 1.CC00” on page 129) and the corresponding mask register (see “PMA Transmit Vendor Interrupt Mask 1: Address 1.D400” on page 132). |
| E | Vendor Specific TX Alarms 2 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “PMA Transmit Vendor Alarms 2: Address 1.CC01” on page 129) and the corresponding mask register (see “PMA Transmit Vendor Interrupt Mask 2: Address 1.D401” on page 132). |
| D | Vendor Specific TX Alarms 3 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “PMA Transmit Vendor Alarms 3: Address 1.CC02” on page 130) and the corresponding mask register (see “PMA Transmit Vendor Interrupt Mask 3: Address 1.D402” on page 133). |

*Table 6.6.59* **PMA Vendor Global Interrupt Flags 1: Address 1.FC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| B | Standard Alarm 1 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from bit 1.1.2. An interrupt was generated from status register (see “PMA Standard Status 1: Address 1.1” on page 2) and the corresponding mask register (see “PMA Transmit Standard Interrupt Mask 1: Address 1.D000” on page 131). |
| A | Standard Alarm 2 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from either bit 1.8.B or 1.8.A. An interrupt was generated from status register (see “PMA Standard Status 2: Address 1.8” on page 8) and the corresponding mask register (see “PMA Transmit Standard Interrupt Mask 2: Address 1.D001” on page 131). |

*Table 6.6.59* **PMA Vendor Global Interrupt Flags 1: Address 1.FC00** (continued)

# 6.7 PCS Registers

### 6.7.1 PCS Standard Control 1: Address 3.0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reset | 1 = PCS reset<br>0 = Normal operation | R/W SC | 1 | Resets the entire PHY, and the reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. This bit is set to 1 during reset. The reset is internally stretched by approximately 1.7 µs. Therefore the MDIO or uP should allow for 1.7 µs before writing any PCS registers after this bit is set. |
| E | Loopback | 1 = Enables loopback mode<br>0 = Normal operation | R/W PD | 0 | This enables the PCS DSQ System Loopback.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| D | Speed Selection LSB | {6,D}<br>1 1 = Speed set by Bits [5:2]<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s | R/W PD | 1 | |
| C | Reserved_0a | Reserved bit 12 | R/W PD | 0 | |
| B | Low Power | 1 = Low-power mode<br>0 = Normal operation | R/W PD | 0 | A 1 written to this register causes the PCS to enter low-power mode. If a global chip low-power state is desired, set Bit B in "Global Standard Control 1: Address 1E.0".<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.7.1* **PCS Standard Control 1: Address 3.0**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A | Clock Stop Enable | 1 = The PHY may stop the clock during LPI<br>0 = Clock *not* stoppable | R/W PD | 0 | |
| 9:7 | Reserved_0b [9:7] | Reserved bits [9:7] | R/W PD | 0x0 | |
| 6 | Speed Selection MSB | {6,D}<br>1 1 = Speed set by Bits [5:2]<br>1 0 = 1000 Mb/s<br>0 1 = 100 Mb/s<br>0 0 = 10 Mb/s | R/W PD | 1 | |
| 5:2 | 10G Speed Selection [3:0] | 1 1 x x = Reserved<br>1 0 1 x = Reserved<br>1 0 0 1 = Reserved<br>0 1 0 0 = 100 Gb/s<br>0 0 1 1 = 40 Gb/s<br>0 0 0 1 = 10PASS-TS / 2BASE-TL<br>0 0 0 0 = 10 Gb/s<br>1 0 0 0 = 5 Gb/s<br>0 1 1 1 = 2.5Gb/s | R/W PD | 0x0 | |
| 1:0 | Reserved_0c [1:0] | Reserved bits [1:0] | R/W PD | 0x0 | |

*Table 6.7.1* **PCS Standard Control 1: Address 3.0** (continued)

### 6.7.2 PCS Standard Status 1: Address 3.1

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved_01a [F:C] | Reserved bits [15:12] | R/W | 0x0 | |
| B | TX LPI Received | 1 = TX PCS has received LPI<br>0 = LPI *not* received | LH | | Source of the LPI signal is configured in 1E.C4A2.4:0. |
| A | RX LPI Received | 1 = RX PCS has received LPI<br>0 = LPI *not* received | LH | | Source of the LPI signal is configured in 1E.C4A1.4:0. |
| 9 | TX LPI Indication | 1 = TX PCS is currently receiving LPI<br>0 = TX PCS is *not* currently receiving LPI | RO | | Source of the LPI signal is configured in 1E.C4A2.4:0. |
| 8 | RX LPI Indication | 1 = RX PCS is currently receiving LPI<br>0 = RX PCS is *not* currently receiving LPI | RO | | Source of the LPI signal is configured in 1E.C4A1.4:0. |
| 7 | Fault | 1 = Fault condition detected<br>0 = No fault detected | RO | | Top-level fault indicator flag for the PCS block. This bit is set if either of the two bits, 3.8.B or 3.8.A,are set. |
| 6 | Clock Stop Capable | 1 = The MAC may stop the clock during LPI<br>0 = Clock *not* stoppable | ROS | 0 | |
| 5:3 | Reserved_01b [5:3] | Reserved bits [5:3] | R/W | 0x0 | |
| 2 | PCS Receive Link Status | Status of the PCS receive link<br>1 = Link up<br>0 = Link lost since last read | LL | | Indicates the status of the PCS receive link. This is a latching-low version of Bit 3.20.C. |

*Table 6.7.2* **PCS Standard Status 1: Address 3.1**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | Low Power Ability | 1 = PCS supports low-power mode<br>0 = No low-power mode supported | ROS | 1 | Indicates whether the XAUI interface supports a low-power mode. |
| 0 | Reserved_01c | Reserved bit 0 | R/W | 0 | |

*Table 6.7.2* **PCS Standard Status 1: Address 3.1** (continued)

### 6.7.3 PCS Standard Device Identifier 1: Address 3.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.7.3* **PCS Standard Device Identifier 1: Address 3.2**

### 6.7.4 PCS Standard Device Identifier 2: Address 3.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.7.4* **PCS Standard Device Identifier 2: Address 3.3**

### 6.7.5 PCS Standard Speed Ability: Address 3.4

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved_4a [F:8] | Reserved bits [15:8] | ROS | 0x00 | |
| 7 | 5G Capable | 1 = PCS is 5 Gb/s capable<br>0 = PCS is *not* 5 Gb/s capable | ROS | 1 | |
| 6 | 2.5G Capable | 1 = PCS is 2.5 Gb/s capable<br>0 = PCS is *not* 2.5 Gb/s capable | ROS | 1 | |
| 5:2 | Reserved_4b [5:2] | Reserved bits [5:2] | ROS | 0x0 | |
| 1 | 10PASS-TS / 2BASE-TL Capable | 1 = PCS is 10PASS-TS/2BASE-TL capable<br>0 = PCS is *not* 10PASS-TS / 2BASE-TL capable | ROS | 0 | |
| 0 | 10G Capable | 1 = PCS is 10 Gb/s capable<br>0 = PCS is *not* 10 Gb/s capable | ROS | 1 | |

*Table 6.7.5* **PCS Standard Speed Ability: Address 3.4**

### 6.7.6 PCS Standard Devices in Package 1: Address 3.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as Autonegotiation is present in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |

*Table 6.7.6* **PCS Standard Devices in Package 1: Address 3.5**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no DTE XAUI interface in the AQR107-AQR109. |
| 4 | PHY XS Present | 1 = PHY XS is present in package<br>0 = PHY XS is *not* present in package | ROS | 1 | Always set to 1 as there is a PHY XS interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1 as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1 as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.7.6* **PCS Standard Devices in Package 1: Address 3.5** (continued)

### 6.7.7 PCS Standard Devices in Package 2: Address 3.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the global control registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the GbE registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.7* **PCS Standard Devices in Package 2: Address 3.6**

### 6.7.8 PCS Standard Control 2: Address 3.7

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved_7 [F:4] | Reserved bits [15:4] | R/W PD | 0x000 | |
| 3:0 | PCS Device Type [3:0] | 0xC to 0xF = Reserved<br>0xB = 5GBASE-T<br>0xA = 2.5GBASE-T<br>0x4 to 0x9 = Reserved<br>0x3 = 10GBASE-T<br>0x2 = 10GBASE-W<br>0x1 = 10GBASE-X<br>0x0 = 10GBASE-R | R/W PD | 0x3 | Defaults to 10GBASE-T. |

*Table 6.7.8* **PCS Standard Control 2: Address 3.7**

### 6.7.9 PCS Standard Status 2: Address 3.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 0x2, as the PCS registers reside here in the AQR107-AQR109. |
| D | 5GBASE-T capable | 1 = PCS supports 5GBASE-T PCS type<br>0 = PCS does *not* support 5GBASE-T | ROS | 1 | Field is always set to 1, as the PCS in the AQR107-AQR109 only supports 5GBASE-T. |
| C | 2.5GBASE-T capable | 1 = PCS supports 2.5GBASE-T PCS type<br>0 = PCS does *not* support 2.5GBASE-T | ROS | 1 | Field is always set to 1, as PCS in the AQR107-AQR109 only supports 2.5GBASE-T. |
| B | Transmit Fault | 1 = Fault condition on transmit path<br>0 = No fault condition on transmit path | LH | | Bit indicates if there is a fault somewhere along the transmit path. This bit is duplicated at 3.CC01.0. |
| A | Receive Fault | 1 = Fault condition on receive path<br>0 = No fault condition on receive path | LH | | Bit indicates if there is a fault somewhere along the receive path. This bit is duplicated at 3.EC04.2. |
| 9:4 | Reserved_8 [9:4] | Reserved bits [9:4] | R/W PD | 0x00 | |
| 3 | 10GBASE-T capable | 1 = PCS supports 10GBASE-T PCS type<br>0 = PCS does *not* support 10GBASE-T | ROS | 1 | Field is always set to 1, as the PCS in the AQR107-AQR109 only supports 10GBASE-T and 10GBASE-R. |
| 2 | 10GBASE-W capable | 1 = PCS supports 10GBASE-W PCS type<br>0 = PCS does *not* support 10GBASE-W | ROS | 0 | Field is always set to 0, as the PCS in the AQR107-AQR109 only supports 10GBASE-T and 10GBASE-R. |

*Table 6.7.9* **PCS Standard Status 2: Address 3.8**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | 10GBASE-X capable | 1 = PCS supports 10GBASE-X PCS type<br>0 = PCS does *not* support 10GBASE-X | ROS | 0 | Field is always set to 0, as the PCS in the AQR107-AQR109 only supports 10GBASE-T and 10GBASE-R. |
| 0 | 10GBASE-R capable | 1 = PCS supports 10GBASE-R PCS type<br>0 = PCS does *not* support 10GBASE-R | ROS | 1 | Field is always set to 1, as the PCS in the AQR107-AQR109 only supports 10GBASE-T and 10GBASE-R. |

*Table 6.7.9* **PCS Standard Status 2: Address 3.8** (continued)

### 6.7.10 PCS Standard Package Identifier 1: Address 3.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31- 16 of Package ID | RO | | |

*Table 6.7.10* **PCS Standard Package Identifier 1: Address 3.E**

### 6.7.11 PCS Standard Package Identifier 2: Address 3.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15 - 0 of Package ID | RO | | |

*Table 6.7.11* **PCS Standard Package Identifier 2: Address 3.F**

### 6.7.12 PCS EEE Capability Register: Address 3.14

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | 10GBASE-KR EEE | 1 = Advertise that the 10GBASE-KR has EEE capability<br>0 = Do *not* advertise that the 10GBASE-KR has EEE capability | ROS | 1 | |
| 5 | 10GBASE-KX4 EEE | 1 = Advertise that the 10GBASE-KX4 has EEE capability<br>0 = Do *not* advertise that the 10GBASE-KX4 has EEE capability | ROS | 1 | |
| 4 | 1000BASE-KX EEE | 1 = Advertise that the 1000BASE-KX has EEE capability<br>0 = Do *not* advertise that the 1000BASE-KX has EEE capability | ROS | 1 | |
| 3 | 10GBASE-T EEE | 1 = Advertise that the 10GBASE-T has EEE capability<br>0 = Do *not* advertise that the 10GBASE-T has EEE capability | ROS | 1 | |
| 2 | 1000BASE-T EEE | 1 = Advertise that the 1000BASE-T has EEE capability<br>0 = Do *not* advertise that the 1000BASE-T has EEE capability | ROS | 1 | |
| 1 | 100BASE-TX EEE | 1 = Advertise that the 100BASE-TX has EEE capability<br>0 = Do *not* advertise that the 100BASE-TX has EEE capability | ROS | 0 | |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.12* **PCS EEE Capability Register: Address 3.14**

### 6.7.13 PCS EEE Capability 2 Register: Address 3.15

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved_15 [F:2] | Reserved bits [15:2] | R/W PD | 0x0000 | |
| 1 | 5GBASE-T EEE | 1 = Advertise that the 5GBASE-T has EEE capability<br>0 = Do *not* advertise that the 5GBASE-T has EEE capability | ROS | 1 | |
| 0 | 2.5GBASE-T EEE | 1 = Advertise that the 2.5GBASE-T has EEE capability<br>0 = Do *not* advertise that the 2.5GBASE-T has EEE capability | ROS | 1 | |

*Table 6.7.13* **PCS EEE Capability 2 Register: Address 3.15**

### 6.7.14 PCS EEE Wake Error Counter: Address 3.16

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | EEE Wake Error Counter [F:0] | EEE wake error counter | SCT | 0x0000 | Register is a 16-bit saturating clear on read counter. The wake error source is configured with 1E.C4A3.2:0. The default wake error source is from the RPL. |

*Table 6.7.14* **PCS EEE Wake Error Counter: Address 3.16**

### 6.7.15 PCS Reserved 17 Register: Address 3.17

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_17 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.15* **PCS Reserved 17 Register: Address 3.17**

### 6.7.16 PCS Reserved 18 Register: Address 3.18

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_18 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.16* **PCS Reserved 18 Register: Address 3.18**

### 6.7.17 PCS Reserved 19 Register: Address 3.19

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_19 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.17* **PCS Reserved 19 Register: Address 3.19**

### 6.7.18 PCS Reserved 1A Register: Address 3.1A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_1A [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.18* **PCS Reserved 1A Register: Address 3.1A**

### 6.7.19 PCS 10G Status 1: Address 3.20

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Reserved_20a [F:D] | Reserved bits [15:13] | ROS | 0x0 | |
| C | 10G Receive Link Status | 1 = 10G Receive Link Up<br>0 = 10G Receive Link Down | RO | | When set, bit indicates that the 10G Receive Link is functioning properly. This is a non-latching version of bit 3.1.2. see “PCS Standard Status 1: Address 3.1” on page 173 The Receive Link is up when the Block Lock status is asserted (and the High BER is deasserted). |
| B:4 | Reserved_20b [B:4] | Reserved bits [11:4] | ROS | 0x00 | |
| 3 | 10GBASE-R PRBS9 Pattern Testing Ability | 1 = PCS is able to support PRBS9 pattern testing on KR Interface<br>0 = PCS is *not* able to support PRBS9 pattern testing on KR Interface | ROS | 1 | |
| 2 | 10GBASE-R PRBS31 Pattern Testing Ability | 1 = PCS is able to support PRBS31 pattern testing on KR Interface<br>0 = PCS is *not* able to support PRBS31 pattern testing on KR Interface | ROS | 1 | |
| 1 | 10G High BER | 1 = PCS is reporting a BER $\geq 10^{-4}$<br>0 = PCS is reporting a BER $< 10^{-4}$ | RO | | When set, bit indicates a high BER is being seen at the PCS. The interrupt for this bit is at 3.21.E. The status bit for medium BER is found in “Global Alarms 2: Address 1E.CC01” on page 572. |
| 0 | 10G PCS Block Lock | 1 = 10GBASE-T PCS Framer is locked<br>0 = 10GBASE-T PCS Framer is *not* locked | RO | | When set, bit indicates that 10G PCS Framer has acquired frame synchronization and is locked. The interrupt for this bit is at 3.21.F. |

*Table 6.7.19* **PCS 10G Status 1: Address 3.20**

### 6.7.20 PCS 10G Status 2: Address 3.21

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PCS Block Lock Latched | 1 = 10GBASE-T PCS Framer is Locked<br>0 = 10GBASE-T PCS Framer is *not* locked | LL | | When set, this bit indicates that 10G PCS Framer has acquired frame synchronization and is locked. This is the interrupt for bit 3.20.0. |
| E | High BER Latched | 1 = PCS is reporting a BER $\geq 10^{-4}$<br>0 = PCS is reporting a BER $< 10^{-4}$ | LH | | When set, this bit indicates a high BER is being seen at the PCS. This is the interrupt for bit 3.20.1.<br><br>The BER counter is a six-bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.18.2.4 for 10/40/100GBASE-R and is defined by the 1fer_count variable in 55.3.6.2 for 10GBASE-T.<br><br>These bits are reset to all zeros when the BASE-R and 10GBASE-T PCS status 2 register is read by the management function or when the PCS reset executes. If the BER high-order counter, 3.44 (see 45.2.3.19) is not implemented, then these bits are held at all ones in the case of overflow. |

*Table 6.7.20* **PCS 10G Status 2: Address 3.21**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D:8 | Errored Frame Counter [5:0] | A saturating count of the number of times a bad LDPC frame is received. | SCT | 0x00 | |
| 7:0 | Errored Block Counter [7:0] | A saturating count of the number of times a bad 65B block is received. | SCT | 0x00 | The errored blocks counter is an eight-bit count defined by the errored_block counter specified in 49.2.14.2 for 10GBASE-R, in 82.3.1 for 40/100GBASE-R and defined by the errored_block_count variable in 55.3.6.2 for 10GBASE-T. These bits are reset to all zeros when the errored blocks count is read by the management function or when the PCS reset executes. If the errored blocks high-order counter, 3.45 (see 45.2.3.20) is not implemented, then these bits are held at all ones in case of overflow. |

*Table 6.7.20* **PCS 10G Status 2: Address 3.21** (continued)

### 6.7.21 PCS 10GBASE-R Test Pattern Seed A 1: Address 3.22

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed A Bits 15:0 [F:0] | Test pattern seed A bits 15:0 | R/W PD | 0x0000 | |

*Table 6.7.21* **PCS 10GBASE-R Test Pattern Seed A 1: Address 3.22**

### 6.7.22 PCS 10GBASE-R Test Pattern Seed A 2: Address 3.23

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed A Bits 31:16 [1F:10] | Test pattern seed A bits 31:16 | R/W PD | 0x0000 | |

*Table 6.7.22* **PCS 10GBASE-R Test Pattern Seed A 2: Address 3.23**

### 6.7.23 PCS 10GBASE-R Test Pattern Seed A 3: Address 3.24

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed A Bits 47:32 [2F:20] | Test pattern seed A bits 47:32 | R/W PD | 0x0000 | |

*Table 6.7.23* **PCS 10GBASE-R Test Pattern Seed A 3: Address 3.24**

### 6.7.24 PCS 10GBASE-R Test Pattern Seed A 4: Address 3.25

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | Test Pattern Seed A Bits 57:48 [39:30] | Test pattern seed A bits 57:48 | R/W PD | 0x000 | |

*Table 6.7.24* **PCS 10GBASE-R Test Pattern Seed A 4: Address 3.25**

### 6.7.25 PCS 10GBASE-R Test Pattern Seed B 1: Address 3.26

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed B Bits 15:0 [F:0] | Test pattern seed B bits 15:0 | R/W PD | 0x0000 | |

*Table 6.7.25* **PCS 10GBASE-R Test Pattern Seed B 1: Address 3.26**

### 6.7.26 PCS 10GBASE-R Test Pattern Seed B 2: Address 3.27

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed B Bits 31:16 [1F:10] | Test pattern seed B bits 31:16 | R/W PD | 0x0000 | |

*Table 6.7.26* **PCS 10GBASE-R Test Pattern Seed B 2: Address 3.27**

### 6.7.27 PCS 10GBASE-R Test Pattern Seed B 3: Address 3.28

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Seed B Bits 47:32 [2F:20] | Test pattern seed B bits 47:32 | R/W PD | 0x0000 | |

*Table 6.7.27* **PCS 10GBASE-R Test Pattern Seed B 3: Address 3.28**

### 6.7.28 PCS 10GBASE-R Test Pattern Seed B 4: Address 3.29

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | Test Pattern Seed B Bits 57:48 [39:30] | Test pattern seed B bits 57:48 | R/W PD | 0x000 | |

*Table 6.7.28* **PCS 10GBASE-R Test Pattern Seed B 4: Address 3.29**

### 6.7.29 PCS 10GBASE-R PCS Test-Pattern Control: Address 3.2A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | PRBS9 Transmit Test-Pattern Enable | 1 = Enables PRBS9 test-pattern mode on the transmit path<br>0 = Disables PRBS9 test-pattern mode on the transmit path | R/W PD | 0 | |
| 5 | PRBS31 Receive Test-Pattern Enable | 1 = Enables PRBS31 test-pattern mode on the receive path<br>0 = Enables PRBS31 test-pattern mode on the receive path | R/W PD | 0 | |
| 4 | PRBS31 Transmit Test-Pattern Enable | 1 = Enables PRBS31 test-pattern mode on the transmit path<br>0 = Enables PRBS31 test-pattern mode on the transmit path | R/W PD | 0 | |
| 3 | Transmit Test-Pattern Enable | 1 = Enables transmit test pattern<br>0 = Disables transmit test pattern | R/W PD | 0 | |

*Table 6.7.29* **PCS 10GBASE-R PCS Test-Pattern Control: Address 3.2A**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Receive Test-Pattern Enable | 1 = Enables receive test-pattern testing<br>0 = Disable receive test-pattern testing | R/W PD | 0 | |
| 1 | Test-Pattern Select | 1 = Square wave test pattern<br>0 = Pseudo random test pattern | R/W PD | 0 | |
| 0 | Data Pattern Select | 1 = Zeros data pattern<br>0 = LF data pattern | R/W PD | 0 | |

*Table 6.7.29* **PCS 10GBASE-R PCS Test-Pattern Control: Address 3.2A** (continued)

### 6.7.30 PCS 10GBASE-R PCS Test-Pattern Error Counter: Address 3.2B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test-Pattern Error Counter [F:0] | Error Counter | R/W PD | 0x0000 | |

*Table 6.7.30* **PCS 10GBASE-R PCS Test-Pattern Error Counter: Address 3.2B**

### 6.7.31 PCS Reserved 2E Register: Address 3.2E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_2E [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.31* **PCS Reserved 2E Register: Address 3.2E**

### 6.7.32 PCS Reserved 2F Register: Address 3.2F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_2F [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.32* **PCS Reserved 2F Register: Address 3.2F**

### 6.7.33 PCS Reserved 30 Register: Address 3.30

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_30 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.33* **PCS Reserved 30 Register: Address 3.30**

### 6.7.34 PCS Reserved 31 Register: Address 3.31

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_31 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.7.34* **PCS Reserved 31 Register: Address 3.31**

### 6.7.35 TimeSync PCS Capability: Address 3.708

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | TimeSync Transmit Path Data Delay | 1 = PCS provides information on transmit path data delay in registers 3.1801 through 3.1804<br>0 = PCS does *not* provide information on transmit path data delay | RO | | |
| 0 | TimeSync Receive Path Data Delay | 1 = PCS provides information on receive path data delay in registers 3.1805 through 3.1808<br>0 = PCS does *not* provide information on receive path data delay | RO | | |

*Table 6.7.35* **TimeSync PCS Capability: Address 3.708**

### 6.7.36 TimeSync PCS Transmit Path Data Delay 1: Address 3.709

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PCS Transmit Path Data Delay LSW [F:0] | LSW of maximum PCS transmit delay in nanoseconds | RO | | |

*Table 6.7.36* **TimeSync PCS Transmit Path Data Delay 1: Address 3.709**

### 6.7.37 TimeSync PCS Transmit Path Data Delay 2: Address 3.70A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PCS Transmit Path Data Delay MSW [F:0] | MSW of maximum PCS transmit delay in nanoseconds | RO | | |

*Table 6.7.37* **TimeSync PCS Transmit Path Data Delay 2: Address 3.70A**

### 6.7.38 TimeSync PCS Transmit Path Data Delay 3: Address 3.70B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PCS Transmit Path Data Delay LSW [F:0] | LSW of minimum PCS transmit delay in nanoseconds | RO | | |

*Table 6.7.38* **TimeSync PCS Transmit Path Data Delay 3: Address 3.70B**

### 6.7.39 TimeSync PCS Transmit Path Data Delay 4: Address 3.70C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PCS Transmit Path Data Delay MSW [F:0] | MSW of minimum PCS transmit delay in nanoseconds | RO | | |

*Table 6.7.39* **TimeSync PCS Transmit Path Data Delay 4: Address 3.70C**

### 6.7.40 TimeSync PCS Receive Path Data Delay 1: Address 3.70D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PCS Receive Path Data Delay LSW [F:0] | LSW of maximum PCS receive delay in nanoseconds | RO | | |

*Table 6.7.40* **TimeSync PCS Receive Path Data Delay 1: Address 3.70D**

### 6.7.41 TimeSync PCS Receive Path Data Delay 2: Address 3.70E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PCS Receive Path Data Delay MSW [F:0] | MSW of maximum PCS receive delay in nanoseconds | RO | | |

*Table 6.7.41* **TimeSync PCS Receive Path Data Delay 2: Address 3.70E**

### 6.7.42 TimeSync PCS Receive Path Data Delay 3: Address 3.70F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PCS Receive Path Data Delay LSW [F:0] | LSW of minimum PCS receive delay in nanoseconds | RO | | |

*Table 6.7.42* **TimeSync PCS Receive Path Data Delay 3: Address 3.70F**

### 6.7.43 TimeSync PCS Receive Path Data Delay 4: Address 3.710

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PCS Receive Path Data Delay MSW [F:0] | MSW of minimum PCS receive delay in nanoseconds | RO | | |

*Table 6.7.43* **TimeSync PCS Receive Path Data Delay 4: Address 3.710**

### 6.7.44 PCS Transmit Vendor Provisioning 1: Address 3.C400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PCS TX Auxiliary Bit Value | The value that will be set in the auxiliary bit of the PCS transmission frame | R/W PD | 0 | Bit is currently undefined in the 802.3an standard. |

*Table 6.7.44* **PCS Transmit Vendor Provisioning 1: Address 3.C400**

### 6.7.45 PCS Transmit Vendor Provisioning 2: Address 3.C401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.45* **PCS Transmit Vendor Provisioning 2: Address 3.C401**

### 6.7.46 PCS Transmit Reserved Vendor Provisioning 1: Address 3.C410

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved Transmit Provisioning 1 [F:1] | Reserved for future use | R/W PD | 0x0000 | |
| 0 | PCS IEEE Loopback Passthrough Disable | 1 = Disables data passthrough on IEEE loopback | R/W PD | 0 | When set, bit disables the output of the PHY when IEEE loopback is set. |

*Table 6.7.46* **PCS Transmit Reserved Vendor Provisioning 1: Address 3.C410**

### 6.7.47 PCS Transmit XFI Vendor Provisioning 1: Address 3.C455

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed A Word 0 [F:0] | XFI test pattern seed A bits 15:0 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed A |

*Table 6.7.47* **PCS Transmit XFI Vendor Provisioning 1: Address 3.C455**

### 6.7.48 PCS Transmit XFI Vendor Provisioning 2: Address 3.C456

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed A Word 1 [F:0] | XFI test pattern seed A bits 31:16 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed A |

*Table 6.7.48* **PCS Transmit XFI Vendor Provisioning 2: Address 3.C456**

### 6.7.49 PCS Transmit XFI Vendor Provisioning 3: Address 3.C457

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed A Word 2 [F:0] | XFI test pattern seed A bits 47:32 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed A |

*Table 6.7.49* **PCS Transmit XFI Vendor Provisioning 3: Address 3.C457**

### 6.7.50 PCS Transmit XFI Vendor Provisioning 4: Address 3.C458

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI Test Pattern Seed A Word 3 [9:0] | XFI test pattern seed A bits 57:48 | R/W | 0x000 | 10GBASE-R Test Pattern Seed A |

*Table 6.7.50* **PCS Transmit XFI Vendor Provisioning 4: Address 3.C458**

### 6.7.51 PCS Transmit XFI Vendor Provisioning 5: Address 3.C459

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed B Word 0 [F:0] | XFI test pattern seed B bits 15:0 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed B |

*Table 6.7.51* **PCS Transmit XFI Vendor Provisioning 5: Address 3.C459**

### 6.7.52 PCS Transmit XFI Vendor Provisioning 6: Address 3.C45A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed B Word 1 [F:0] | XFI test pattern seed B bits 31:16 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed B |

*Table 6.7.52* **PCS Transmit XFI Vendor Provisioning 6: Address 3.C45A**

### 6.7.53 PCS Transmit XFI Vendor Provisioning 7: Address 3.C45B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI Test Pattern Seed B Word 2 [F:0] | XFI test pattern seed B bits 47:32 | R/W | 0x0000 | 10GBASE-R Test Pattern Seed B |

*Table 6.7.53* **PCS Transmit XFI Vendor Provisioning 7: Address 3.C45B**

### 6.7.54 PCS Transmit XFI Vendor Provisioning 8: Address 3.C45C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI Test Pattern Seed B Word 3 [9:0] | XFI test pattern seed B bits 57:48 | R/W | 0x000 | 10GBASE-R Test Pattern Seed B |

*Table 6.7.54* **PCS Transmit XFI Vendor Provisioning 8: Address 3.C45C**

### 6.7.55 PCS Transmit XFI0 Vendor Provisioning 1: Address 3.C460

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | XFI0 PCS Scrambler Disable | 1 = Disables PCS scrambler | R/W PD | 0 | PCS Scrambler Disable (default: 0) |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.55* **PCS Transmit XFI0 Vendor Provisioning 1: Address 3.C460**

### 6.7.56 PCS Transmit XFI0 Vendor Provisioning 2: Address 3.C461

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9 | XFI0 Test Square Wave Test Duration | 0 = 6 ones followed by 6 zeros<br>1 = 11 ones followed by 11 zeroed | R/W | 0 | 10GBASE-R Square Wave Test Duration. Repeating pattern of *n* ones, followed by *n* zeros, where *n* = 6 or 11 (0: n = 6, 1: n =11, default: 0). |
| 8 | XFI0 Test Data Select | 1 = Data pattern select | R/W | 0 | 10GBASE-R Data Pattern Select (0: LF, 1: Zero, default: 0). |
| 7 | XFI0 Test Mode Select | 1 = Test pattern select | R/W | 0 | 10GBASE-R Test Pattern Select (0: Pseudo random, 1: Square wave, default: 0). |
| 6 | XFI0 Test PRBS-9 Enable | 1 = Test pattern PRBS-9 enabled | R/W | 0 | 10GBASE-R PRBS 9 Test Pattern Enable (0: disable, 1: enable, default: 0). |
| 5 | XFI0 Test PRBS-31 Enable | 1 = Test pattern PRBS-31 enabled | R/W | 0 | 10GBASE-R PRBS 31 Test Pattern Enable (0: disable, 1: enable, default: 0). |

*Table 6.7.56* **PCS Transmit XFI0 Vendor Provisioning 2: Address 3.C461**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | XFI0 Test Pattern Enable | 1 = Test pattern enabled | R/W | 0 | 10GBASE-R Pseudo-Random Test Pattern Enable (0: disable, 1: enable, default: 0). |
| 3 | XFI0 Local Fault Inject | 1 = Inject local fault | R/W | 0 | Inject Local_Fault (default: 0). |
| 2 | XFI0 Inject Single Error | 1 = Inject single Error | R/W | 0 | Inject single error on the 10GBASE-R Test Pattern including pseudo-random, PRB31 or PRBS9 (default: 0). |
| 1 | XFI0 PCS High BER Inject | 1 = Inject PCS High BER | R/W | 0 | Inject error to cause HI_BER at far-end (default: 0). |
| 0 | XFI0 PCS Loss Of Lock Inject | 1 = Inject loss of lock | R/W | 0 | Inject error to cause loss of block_lock at far-end (default: 0). |

*Table 6.7.56* **PCS Transmit XFI0 Vendor Provisioning 2: Address 3.C461** (continued)

### 6.7.57 PCS Transmit XFI1 Vendor Provisioning 1: Address 3.C470

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.57* **PCS Transmit XFI1 Vendor Provisioning 1: Address 3.C470**

### 6.7.58 PCS Transmit XFI1 Vendor Provisioning 2: Address 3.C471

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.58* **PCS Transmit XFI1 Vendor Provisioning 2: Address 3.C471**

### 6.7.59 PCS SerDes MUX Swap TXRX Register: Address 3.C4F0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | SerDes Mux Swap TX Lane 3 [1:0] | The lane swap setting for Lane 3, in the TX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 3, 1 = lane 0, 2 = lane 1, 3 = lane 2 |
| D:C | SerDes Mux Swap TX Lane 2 [1:0] | The lane swap setting for Lane 2, in the TX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 2, 1 = lane 3, 2 = lane 0, 3 = lane 1 |
| B:A | Serdes Mux Swap TX Lane 1 [1:0] | The lane swap setting for Lane 1, in the TX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 1, 1 = lane 2, 2 = lane 3, 3 = lane 0 |
| 9:8 | Serdes Mux Swap TX Lane 0 [1:0] | The lane swap setting for Lane 0, in the TX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 0, 1 = lane 1, 2 = lane 2, 3 = lane 3 |
| 7:6 | Serdes Mux Swap RX Lane 3 [1:0] | The lane swap setting for Lane 3, in the RX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 3, 1 = lane 0, 2 = lane 1, 3 = lane 2 |
| 5:4 | Serdes Mux Swap RX Lane 2 [1:0] | The lane swap setting for Lane 2, in the RX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 2, 1 = lane 3, 2 = lane 0, 3 = lane 1 |

*Table 6.7.59* **PCS SerDes MUX Swap TXRX Register: Address 3.C4F0**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3:2 | Serdes Mux Swap RX Lane 1 [1:0] | The lane swap setting for Lane 1, in the RX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 1, 1 = lane 2, 2 = lane 3, 3 = lane 0 |
| 1:0 | Serdes Mux Swap RX Lane 0 [1:0] | The lane swap setting for Lane 0, in the RX direction (implemented at the internal interface between the SerDes and digital logic) | R/W | 0x0 | 0 = lane 0, 1 = lane 1, 2 = lane 2, 3 = lane 3 |

*Table 6.7.59* **PCS SerDes MUX Swap TXRX Register: Address 3.C4F0** (continued)

### 6.7.60 PCS Transmit TPL Timestamp Counter 0: Address 3.C548

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TPL Egress Average Timestamp Counter [F:0] | TPL Egress Average or Current Timestamp counter | RO | | When configured to perform averaging, it returns the averaging value of the timestamp difference between the insertion and removal points. Otherwise, it returns the current value of the timestamp difference. |

*Table 6.7.60* **PCS Transmit TPL Timestamp Counter 0: Address 3.C548**

### 6.7.61 PCS Transmit TPL Timestamp Counter 1: Address 3.C549

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TPL Egress Max Timestamp Counter [F:0] | TPL Egress Max Timestamp counter | RO | | Returns the maximum value of the timestamp difference between the insertion and removal points. |

*Table 6.7.61* **PCS Transmit TPL Timestamp Counter 1: Address 3.C549**

### 6.7.62 PCS Transmit TPL Timestamp Counter 2: Address 3.C54A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TPL Egress Min Timestamp Counter [F:0] | TPL Egress Min Timestamp counter | RO | | Returns the minimum value of the timestamp difference between the insertion and removal points. |

*Table 6.7.62* **PCS Transmit TPL Timestamp Counter 2: Address 3.C54A**

### 6.7.63 PCS Transmit TGE Vendor Timestamp Counter 0: Address 3.C568

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TGE Egress Average Timestamp Counter [F:0] | TGE Egress Average or Current Timestamp counter | RO | | When configured to perform averaging, it returns the averaging value of the timestamp difference between the insertion and removal points. Otherwise, it returns the current value of the timestamp difference. |

*Table 6.7.63* **PCS Transmit TGE Vendor Timestamp Counter 0: Address 3.C568**

### 6.7.64 PCS Transmit TGE Vendor Timestamp Counter 1: Address 3.C569

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TGE Egress Max Timestamp Counter [F:0] | TGE Egress Max Timestamp counter | RO | | Returns the maximum value of the timestamp difference between the insertion and removal points. |

*Table 6.7.64* **PCS Transmit TGE Vendor Timestamp Counter 1: Address 3.C569**

### 6.7.65 PCS Transmit TGE Vendor Timestamp Counter 2: Address 3.C56A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | TGE Egress Min Timestamp Counter [F:0] | TGE Egress Min Timestamp counter | RO | | Returns the minimum value of the timestamp difference between the insertion and removal points. |

*Table 6.7.65* **PCS Transmit TGE Vendor Timestamp Counter 2: Address 3.C56A**

### 6.7.66 PCS PTP Egress Vendor Provisioning 1: Address 3.C620

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PTP Egress VLAN Tagging Enable | 1 = PTP Egress VLAN tagging enabled | R/W | 0 | Enables VLAN tagging for IEEE1588 or NTP/SNTP packet (default: 0x1). |
| E | PTP Egress IPv6/UDP Encapsulated Enabled | 1 = PTP Egress IPv6/UDP encapsulated enabled | R/W | 0 | Enables IPv6/UDP encapsulated IEEE1588 or NTP/SNTP packet (default: 0). |

*Table 6.7.66* **PCS PTP Egress Vendor Provisioning 1: Address 3.C620**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | PTP Egress IPv4/UDP Encapsulated Enabled | 1 = PTP Egress IPv4/UDP encapsulated enable | R/W | 0 | Enables IPv4/UDP encapsulated IEEE1588 or NTP/SNTP packet (default: 0). |
| C | PTP Egress Ethernet Encapsulated Enable | 1 = PTP Egress Ethernet encapsulated enable | R/W | 0 | Enables Ethernet encapsulated IEEE1588 packet (default: 0). |
| B:A | Reserved | Internal reserved - do not modify | | | |
| 9:8 | PTP Egress NTP Configuration [1:0] | PTP Egress NTP/SNTP configuration | R/W | 0x0 | NTP/SNTP configuration (bit 0: 0 = client, 1 = server, bit 1: 0 = egress, 1 = ingress). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | PTP Egress Back Pressure Enable | 1 = PTP Egress back pressure enable | R/W | 0 | PTP FIFO ready enable (default: 0).<br>Set to 1 to enable the back pressure during the appending of timestamp to the end of packet.<br>Set to 0 to disable the back pressure. |
| 4 | PTP Egress NTP Enable | 1 = PTP Egress NTP/SNTP enable | R/W | 0 | Enables NTP/SNTP |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | PTP Egress 1588 Version 2 Enable | 1 = PTP Egress 1588 version 2 enable | R/W | 0 | Enables IEEE 1588 Version 2 |
| 0 | PTP Egress 1588 Version 1 Enable | 1 = PTP Egress 1588 version 1 enable | R/W | 0 | Enables IEEE 1588 Version 1 |

*Table 6.7.66* **PCS PTP Egress Vendor Provisioning 1: Address 3.C620** (continued)

### 6.7.67 PCS PTP Egress Vendor Provisioning 2: Address 3.C621

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | PTP Egress IPv6 Destination Address Matching Enable [2:0] | PTP Egress IPv6 destination address matching enable | R/W | 0x3 | Enables IPv6 destination address matching for IEEE1588 (default:0x3):<br>Bit 0: FF0X:0:0:0:0:0:0:181 (X: 0x0 to 0xF)<br>Bit 1: FF02:0:0:0:0:0:0:6B<br>Bit 2: user-defined |
| B:8 | PTP Egress IPv4 Destination Address Matching Enable [3:0] | PTP Egress IPv4 destination address matching enable | R/W | 0x7 | Enables IPv4 destination address matching for IEEE1588 (default:0x7):<br>Bit 0: 224.0.1.129<br>Bit 1: 224.0.1.130-132<br>Bit 2: 224.0.0.107<br>Bit 3: user-defined |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:4 | PTP Egress MAC Destination Address Matching Enable [2:0] | PTP Egress MAC destination address matching enable | R/W | 0x3 | Enables MAC destination address matching for IEEE1588 (default:0x3):<br>Bit 0: 01-1B-19-00-00-00<br>Bit 1: 01-80-C2-00-00-0E<br>Bit 2: user-defined |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | PTP Egress EtherType Matching Enable [1:0] | PTP Egress EtherType matching enable | R/W | 0x1 | Enables EtherType matching for Ethernet encapsulated IEEE1588 packet (default: 0x1):<br>Bit 0: 0x88F7<br>Bit 1: user-defined<br>This needs to be configured before enabling Ethernet encapsulation (at least one bit needs to be set). |

*Table 6.7.67* **PCS PTP Egress Vendor Provisioning 2: Address 3.C621**

### 6.7.68 PCS PTP Egress Vendor Provisioning 3: Address 3.C622

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | PTP Egress NTP/SNTP Version [2:0] | PTP Egress NTP/SNTP version | R/W | 0x3 | Indicates version of NTP/SNTP (default: 3).<br>Specifies the minimum value of the version number of NTP/SNTP to support. It must *not* be less than 3, and a value of 0 disables version checking. |
| B:8 | PTP Egress 1588 Version [3:0] | PTP Egress IEEE 1588 version | R/W | 0x2 | Indicates latest version of IEEE1588 (default: 2).<br>Allows support of future versions of the IEEE 1588. It must *not* be less than 2, and a value of 0 disables version checking and it assumes it is compatible with version 2. |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | PTP Egress 1588 2 Step Enable | PTP Egress 1588 2 step enabled | R/W | 0 | Set to 1 to consider the two-step flag for IEEE1588v2 (or PTP_ASSIST for IEEE1588v1). Prevents timestamp overwriting for 2-step Sync message. Set to 0 allows timestamp update regardless of the flag (default: 0). |
| 4 | PTP Egress 1588 Version 2 Domain Matching Enable | 1 = PTP Egress 1588 version 2 domain matching enabled | R/W | 0 | Enables domain matching for IEEE1588v2 (default: 0). |
| 3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Egress UDP Destination Port Matching Enable [2:0] | PTP Egress UDP destination port matching enabled | R/W | 0x3 | Enabled UDP destination port matching for IEEE 1588 or NTP/SNTP (default:0x3):<br>Bit 0: 319 for IEEE1588, or 123 for NTP/SNTP<br>Bit 1: 320 for IEEE1588, *not* used for NTP/SNTP<br>Bit 2: user-defined |

*Table 6.7.68* **PCS PTP Egress Vendor Provisioning 3: Address 3.C622**

### 6.7.69 PCS PTP Egress Vendor Provisioning 4: Address 3.C623

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress EtherType [F:0] | PTP Egress UDP destination port matching enabled | R/W | 0x0000 | User-defined EtherType for Ethernet encapsulated IEEE1588 packets (default: 0). |

*Table 6.7.69* **PCS PTP Egress Vendor Provisioning 4: Address 3.C623**

### 6.7.70 PCS PTP Egress Vendor Provisioning 5: Address 3.C624

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress MAC Destination Address Bits 15:0 [F:0] | PTP Egress MAC destination address bits 15:0 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.70* **PCS PTP Egress Vendor Provisioning 5: Address 3.C624**

### 6.7.71 PCS PTP Egress Vendor Provisioning 6: Address 3.C625

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress MAC Destination Address Bits 31:16 [1F:10] | PTP Egress MAC destination address bits 31:16 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.71* **PCS PTP Egress Vendor Provisioning 6: Address 3.C625**

### 6.7.72 PCS PTP Egress Vendor Provisioning 7: Address 3.C626

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress MAC Destination Address Bits 47:32 [2F:20] | PTP Egress MAC destination address bits 47:32 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.72* **PCS PTP Egress Vendor Provisioning 7: Address 3.C626**

### 6.7.73 PCS PTP Egress Vendor Provisioning 8: Address 3.C627

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv4 Destination Address LSW [F:0] | PTP Egress IPv4 destination address bits 15:0 | R/W | 0x0000 | User-defined IPv4 destination address (default: 0). |

*Table 6.7.73* **PCS PTP Egress Vendor Provisioning 8: Address 3.C627**

### 6.7.74 PCS PTP Egress Vendor Provisioning 9: Address 3.C628

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv4 Destination Address MSW [1F:10] | PTP Egress IPv4 destination address bits 31:16 | R/W | 0x0000 | User-defined IPv4 destination address (default: 0). |

*Table 6.7.74* **PCS PTP Egress Vendor Provisioning 9: Address 3.C628**

### 6.7.75 PCS PTP Egress Vendor Provisioning 10: Address 3.C629

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 15:0 [F:0] | PTP Egress IPv6 destination address bits 15:0 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.75* **PCS PTP Egress Vendor Provisioning 10: Address 3.C629**

### 6.7.76 PCS PTP Egress Vendor Provisioning 11: Address 3.C62A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 31:16 [1F:10] | PTP Egress IPv6 destination address bits 31:16 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.76* **PCS PTP Egress Vendor Provisioning 11: Address 3.C62A**

### 6.7.77 PCS PTP Egress Vendor Provisioning 12: Address 3.C62B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 47:32 [2F:20] | PTP Egress IPv6 destination address bits 47:32 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.77* **PCS PTP Egress Vendor Provisioning 12: Address 3.C62B**

### 6.7.78 PCS PTP Egress Vendor Provisioning 13: Address 3.C62C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 63:48 [3F:30] | PTP Egress IPv6 destination address bits 63:48 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.78* **PCS PTP Egress Vendor Provisioning 13: Address 3.C62C**

### 6.7.79 PCS PTP Egress Vendor Provisioning 14: Address 3.C62D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 79:64 [4F:40] | PTP Egress IPv6 destination address bits 79:64 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.79* **PCS PTP Egress Vendor Provisioning 14: Address 3.C62D**

### 6.7.80 PCS PTP Egress Vendor Provisioning 15: Address 3.C62E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 95:80 [5F:50] | PTP Egress IPv6 destination address bits 95:80 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.80* **PCS PTP Egress Vendor Provisioning 15: Address 3.C62E**

### 6.7.81 PCS PTP Egress Vendor Provisioning 16: Address 3.C62F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 111:96 [6F:60] | PTP Egress IPv6 destination address bits 111:96 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.81* **PCS PTP Egress Vendor Provisioning 16: Address 3.C62F**

### 6.7.82 PCS PTP Egress Vendor Provisioning 17: Address 3.C630

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress IPv6 Destination Address Bits 127:112 [7F:70] | PTP Egress IPv6 destination address bits 127:112 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.82* **PCS PTP Egress Vendor Provisioning 17: Address 3.C630**

### 6.7.83 PCS PTP Egress Vendor Provisioning 18: Address 3.C631

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress UDP Destination Port [F:0] | PTP Egress UDP destination port | R/W | 0x0000 | User-defined UDP destination port (default: 0). |

*Table 6.7.83* **PCS PTP Egress Vendor Provisioning 18: Address 3.C631**

### 6.7.84 PCS PTP Egress Vendor Provisioning 19: Address 3.C632

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | PTP Egress 1588 Version 2 Domain [7:0] | PTP Egress 1588 Version 2 Domain | R/W | 0x00 | User-defined domain for IEEE1588v2 (default: 0). |

*Table 6.7.84* **PCS PTP Egress Vendor Provisioning 19: Address 3.C632**

### 6.7.85 PCS PTP Egress Vendor Provisioning 20: Address 3.C633

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | PTP Egress Correction Offset Sign | 1 = PTP Egress correction offset sign | R/W | 0 | Correction field offset sign (0: add, 1:subtract, default: 0); indicates whether to add or subtract the correction field offset. |
| 2 | PTP Egress Time Stamp Offset Sign | 1 = PTP Egress time stamp offset sign | R/W | 0 | Timestamp nano-/fractional-seconds offset sign (0: add, 1:subtract, default: 0); indicates whether to add or subtract the timestamp compensation offset. |
| 1 | PTP Egress Set Time Stamp Offset | 1 = PTP Egress set time stamp offset | R/W | 0 | Toggle 0->1->0 to set the new offsets of the timestamp and correction field (default: 0). |
| 0 | PTP Egress Byte Swap | 1 = PTP Egress byte swap | R/W | 0 | Swap byte order of the 32-bit packet data (default: 0). |

*Table 6.7.85* **PCS PTP Egress Vendor Provisioning 20: Address 3.C633**

### 6.7.86 PCS PTP Egress Vendor Provisioning 21: Address 3.C634

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Time Stamp Nanosecond Offset [F:0] | PTP Egress time stamp nanosecond offset | R/W | 0x0000 | Timestamp nanoseconds offset (default: 0); this compensates for the difference between MDI and the timestamping point. |

*Table 6.7.86* **PCS PTP Egress Vendor Provisioning 21: Address 3.C634**

### 6.7.87 PCS PTP Egress Vendor Provisioning 22: Address 3.C635

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Time Stamp Fractional Second Offset LSW [F:0] | PTP Egress time stamp fractional second offset | R/W | 0x0000 | Timestamp fractional-seconds offset (default: 0); which is the LSB 19-bit of the 32-bit fractional-seconds counter. Software checks that this value is equivalent to corresponding nanoseconds offset. |

*Table 6.7.87* **PCS PTP Egress Vendor Provisioning 22: Address 3.C635**

### 6.7.88 PCS PTP Egress Vendor Provisioning 23: Address 3.C636

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Egress Time Stamp Fractional Second Offset MSW [12:10] | PTP Egress time stamp fractional second offset | R/W | 0x0 | Timestamp fractional-seconds offset (default: 0); which is the LSB 19-bit of the 32-bit fractional- seconds counter. Software checks that this value is equivalent to corresponding nanoseconds offset. |

*Table 6.7.88* **PCS PTP Egress Vendor Provisioning 23: Address 3.C636**

### 6.7.89 PCS PTP Egress Vendor Provisioning 24: Address 3.C637

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Correction Offset LSW [F:0] | PTP Egress correction offset | R/W | 0x0000 | Correction field offset (16-bit nanosecond and 16-bit fractional nanosecond, default: 0)<br>This compensates the asymmetrical TX/RX delay, and/or any adjustment for transparent application. |

*Table 6.7.89* **PCS PTP Egress Vendor Provisioning 24: Address 3.C637**

### 6.7.90 PCS PTP Egress Vendor Provisioning 25: Address 3.C638

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Correction Offset MSW [1F:10] | PTP Egress correction offset | R/W | 0x0000 | Correction field offset (16-bit nanosecond and 16-bit fractional nanosecond, default: 0)<br>This compensates the asymmetrical TX/RX delay, and/or any adjustment for transparent application. |

*Table 6.7.90* **PCS PTP Egress Vendor Provisioning 25: Address 3.C638**

### 6.7.91 PCS PTP Egress Vendor Provisioning 26: Address 3.C639

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B:0 | PTP Egress Packet Action [B:0] | PTP Egress packet action | R/W | 0x000 | IEEE 1588v2 packet action(0=None, 1=Capture, 2=reserved, 3=Capture and forward, default: 0)<br>Bits [1:0]: Sync message<br>Bits [3:2]: Delay_Req message<br>Bits [5:4]: Pdelay_Req message<br>Bits [7:6]: Pdelay_Resp message<br>Bits [9:8]: User-defined message<br>Bits [11:10]: General messages |

*Table 6.7.91* **PCS PTP Egress Vendor Provisioning 26: Address 3.C639**

### 6.7.92 PCS PTP Egress Vendor Provisioning 27: Address 3.C63A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:C | PTP Egress NTP/SNTP Time Stamp Action [1:0] | PTP Egress correct action | R/W | 0x0 | NTP/SNTP timestamp action (0=None, 1=Overwrite, 2=Append, 3=reserved) |

*Table 6.7.92* **PCS PTP Egress Vendor Provisioning 27: Address 3.C63A**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| B:8 | PTP Egress NTP/SNTP Packet Action [3:0] | PTP Egress correct action | R/W | 0x0 | NTP/SNTP packet action (0=None, 1=Capture, 2=reserved, 3=Capture and forward, 3=reserved)<br>Bits [1:0]: Non-control messages<br>Bits [3:2]: Control and Private-use messages |
| 7:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.92* **PCS PTP Egress Vendor Provisioning 27: Address 3.C63A**

### 6.7.93 PCS PTP Egress Vendor Provisioning 31: Address 3.C63E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PTP Egress Packet Buffer Reset | 1 = PTP Egress packet buffer reset | R/W | 0 | PTP packet buffer reset (default: 0)<br>Set to 1 to reset PTP packet extraction buffer and timestamp |
| E | PTP USX Timestamp FIFO Reset | 1 = PTP USX timestamp FIFO reset | R/W | 0 | PTP USX timestamp FIFO reset (default: 0)<br>Set to 1 to reset PTP USX timestamp FIFO |
| D:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PTP USX Timestamp FIFO Select | 1 = PTP USX timestamp FIFO select | R/W | 0 | PTP USX timestamp FIFO select (default: 0)<br>Set to 0 to select USX port 0, Set to 1 to select USX port1 |

*Table 6.7.93* **PCS PTP Egress Vendor Provisioning 31: Address 3.C63E**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | PTP USX Timestamp FIFO Read Enable | 1 = PTP USX timestamp FIFO read enable | R/W | 0 | PTP USX timestamp FIFO read (default: 0)<br>Toggle 0->1->0 to read the timestamp out of USX timestamp FIFO |
| 0 | PTP Egress Packet Buffer Read Enable | 1 = PTP Egress packet buffer read enable | R/W | 0 | PTP packet buffer read (default: 0)<br>Toggle 0->1->0 to read the next packet data out of extraction FIFO |

*Table 6.7.93* **PCS PTP Egress Vendor Provisioning 31: Address 3.C63E**

### 6.7.94 PCS PTP Egress Vendor Provisioning 32: Address 3.C63F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | PTP Egress Packet Pause | PTP Egress packet pause | R/W | 0 | PTP packet and timestamp extraction pause (default: 0)<br>Set to 1 to pause the extraction of packet and timestamp into the corresponding buffers. Set to 0 to resume the extraction. |
| 0 | PTP Egress Packet Size Limit | PTP Egress packet size limit | R/W | 0 | PTP packet size limit (default: 0)<br>Set to 1 to limit PTP packet to 128-byte to ensure packet buffer is enough to fit up to 4 packets |

*Table 6.7.94* **PCS PTP Egress Vendor Provisioning 32: Address 3.C63F**

### 6.7.95 PCS PTP Egress Vendor Provisioning 39: Address 3.C646

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3:0 | PTP Egress 1588 Version 2 Message Mask [3:0] | PTP Egress 1588 version 2 message mask | R/W | 0xF | IEEE 1588v2 User-defined Message Mask.<br>Bit mask to compare against the messageType field (for each bit, 1 = compare, 0 = ignore, default: 0xF). |

*Table 6.7.95* **PCS PTP Egress Vendor Provisioning 39: Address 3.C646**

### 6.7.96 PCS Transmit Vendor FCS No Error Frame Counter 1: Address 3.C820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | 10GBASE-T Good Frame Counter LSW [F:0] | 10GBASE-T Good Frame Counter LSW | SCTL | 0x0000 | This counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.96* **PCS Transmit Vendor FCS No Error Frame Counter 1: Address 3.C820**

### 6.7.97 PCS Transmit Vendor FCS No Error Frame Counter 2: Address 3.C821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | 10GBASE-T Good Frame Counter MSW [19:10] | 10GBASE-T Good Frame Counter MSW | SCTM | 0x000 | This counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.97* **PCS Transmit Vendor FCS Error Frame Counter 2: Address 3.C823**

### 6.7.98 PCS Transmit Vendor FCS Error Frame Counter 1: Address 3.C822

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | 10GBASE-T Error Frame Counter LSW [F:0] | 10GBASE-T Bad Frame Counter LSW | SCTL | 0x0000 | This counts Ethernet bad frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.98* **PCS Transmit Vendor FCS Error Frame Counter 1: Address 3.C822**

### 6.7.99 PCS Transmit Vendor FCS Error Frame Counter 2: Address 3.C823

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | 10GBASE-T Error Frame Counter MSW [19:10] | 10GBASE-T Bad Frame Counter MSW | SCTM | 0x000 | This counts Ethernet bad frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.99* **PCS Transmit Vendor FCS Error Frame Counter 2: Address 3.C823**

### 6.7.100 PCS Transmit TPL Vendor State 1: Address 3.C830

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| A:8 | Reserved | Internal reserved - do not modify | | | |
| 7:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | TPL EEE TX LPI State | 1 = TX LPI is currently detected | RO | | Indicates that TX LPI is currently detected. |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | Reserved | Internal reserved - do not modify | | | |
| 0 | TPL EEE TX LPI Active State | 1 = TX LPI is in an Active state | RO | | Indicates that TX LPI is in an Active state. |

*Table 6.7.100* **PCS Transmit TPL Vendor State 1: Address 3.C830**

### 6.7.101 PCS Transmit XFI0 Vendor State 1: Address 3.C860

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI0 Good Frame Counter LSW [F:0] | XFI0 Good Frame Counter LSW | SCTL | 0x0000 | This counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.101* **PCS Transmit XFI0 Vendor State 1: Address 3.C860**

### 6.7.102 PCS Transmit XFI0 Vendor State 2: Address 3.C861

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI0 Good Frame Counter MSW [9:0] | XFI0 Good Frame Counter MSW | SCTM | 0x000 | This counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.102* **PCS Transmit XFI0 Vendor State 2: Address 3.C861**

### 6.7.103 PCS Transmit XFI0 Vendor State 3: Address 3.C862

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI0 Bad Frame Counter LSW [F:0] | XFI0 Bad Frame Counter LSW | SCTL | 0x0000 | This counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.103* **PCS Transmit XFI0 Vendor State 3: Address 3.C862**

### 6.7.104 PCS Transmit XFI0 Vendor State 4: Address 3.C863

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI0 Bad Frame Counter MSW [9:0] | XFI0 Bad Frame Counter MSW | SCTM | 0x000 | This counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.104* **PCS Transmit XFI0 Vendor State 4: Address 3.C863**

### 6.7.105 PCS Transmit XFI1 Vendor State 1: Address 3.C870

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.105* **PCS Transmit XFI1 Vendor State 1: Address 3.C870**

### 6.7.106 PCS Transmit XFI1 Vendor State 2: Address 3.C871

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.106* **PCS Transmit XFI1 Vendor State 2: Address 3.C871**

### 6.7.107 PCS Transmit XFI1 Vendor State 3: Address 3.C872

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.107* **PCS Transmit XFI1 Vendor State 3: Address 3.C872**

### 6.7.108 PCS Transmit XFI1 Vendor State 4: Address 3.C873

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.108* **PCS Transmit XFI1 Vendor State 4: Address 3.C873**

### 6.7.109 PCS Transmit XGS Vendor State 1: Address 3.C880

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XGS Collision Events Counter 0 [7:0] | XGS collision events: Byte location from 1 to 64 bytes counter | SCT | 0x00 | 1G/100M PHY collision events: Byte location from 1 to 64 counter |

*Table 6.7.109* **PCS Transmit XGS Vendor State 1: Address 3.C880**

### 6.7.110 PCS Transmit XGS Vendor State 2: Address 3.C881

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XGS Collision Events Counter 1 [7:0] | XGS collision events: Byte location from 65 to 96 bytes counter | SCT | 0x00 | 1G/100M PHY collision events: Byte location from 65 to 96 counter |

*Table 6.7.110* **PCS Transmit XGS Vendor State 1: Address 3.C880**

### 6.7.111 PCS Transmit XGS Vendor State 3: Address 3.C882

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XGS Collision Events Counter 2 [7:0] | XGS collision events: Byte location from 97 to 128 counter | SCT | 0x00 | 1G/100M PHY collision events: Byte location from 97 to 128 bytes counter |

*Table 6.7.111* **PCS Transmit XGS Vendor State 3: Address 3.C882**

### 6.7.112 PCS Transmit XGS Vendor State 4: Address 3.C883

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XGS Collision Events Counter 3 [7:0] | XGS collision events: Byte location from 129 to 192 counter | SCT | 0x00 | 1G/100M PHY collision events: Byte location from 129 to 192 bytes counter |

*Table 6.7.112* **PCS Transmit XGS Vendor State 4: Address 3.C883**

### 6.7.113 PCS Transmit XGS Vendor State 5: Address 3.C884

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XGS Collision Events Counter 4 [7:0] | XGS collision events: Byte location from 193 to 320 counter | SCT | 0x00 | 1G/100M PHY collision events: Byte location from 193 to 320 bytes counter |

*Table 6.7.113* **PCS Transmit XGS Vendor State 5: Address 3.C884**

### 6.7.114 PCS PTP Vendor State 1: Address 3.C900

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Seconds Count Bits 15:0 [F:0] | PTP digital clock seconds count bits 15:0 | RO | | Digital clock seconds counter current value |

*Table 6.7.114* **PCS PTP Vendor State 1: Address 3.C900**

### 6.7.115 PCS PTP Vendor State 2: Address 3.C901

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Seconds Count Bits 31:16 [1F:10] | PTP digital clock seconds count bits 31:16 | RO | | Digital clock seconds counter current value |

*Table 6.7.115* **PCS PTP Vendor State 2: Address 3.C901**

### 6.7.116 PCS PTP Vendor State 3: Address 3.C902

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Seconds Count Bits 47:32 [2F:20] | PTP digital clock seconds count bits 47:32 | RO | | Digital clock seconds counter current value |

*Table 6.7.116* **PCS PTP Vendor State 3: Address 3.C902**

### 6.7.117 PCS PTP Vendor State 4: Address 3.C903

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Nanoseconds Count LSW [F:0] | PTP digital clock nanoseconds count bits 15:0 | RO | | Digital clock nano-seconds counter current value |

*Table 6.7.117* **PCS PTP Vendor State 4: Address 3.C903**

### 6.7.118 PCS PTP Vendor State 5: Address 3.C904

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Nanoseconds Count MSW [1F:10] | PTP digital clock nanoseconds count bits 31:16 | RO | | Digital clock nano-seconds counter current value |

*Table 6.7.118* **PCS PTP Vendor State 5: Address 3.C904**

### 6.7.119 PCS PTP Vendor State 6: Address 3.C905

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Fractional Nanoseconds Count LSW [F:0] | PTP digital clock fractional nanoseconds count bits 15:0 | RO | | Digital clock fractional nano-seconds counter current value |

*Table 6.7.119* **PCS PTP Vendor State 6: Address 3.C905**

### 6.7.120 PCS PTP Vendor State 7: Address 3.C906

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Fractional Nanoseconds Count MSW [1F:10] | PTP digital clock fractional nanoseconds count bits 31:16 | RO | | Digital clock fractional nano-seconds counter current value |

*Table 6.7.120* **PCS PTP Vendor State 7: Address 3.C906**

### 6.7.121 PCS PTP Vendor State 8: Address 3.C907

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Fractional Seconds Count LSW [F:0] | PTP digital clock fractional seconds count bits 15:0 | RO | | Digital clock fractional seconds counter current value |

*Table 6.7.121* **PCS PTP Vendor State 8: Address 3.C907**

### 6.7.122 PCS PTP Vendor State 9: Address 3.C908

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Digital Clock Fractional Seconds Count MSW [1F:10] | PTP digital clock fractional seconds count bits 31:16 | RO | | Digital clock fractional seconds counter current value |

*Table 6.7.122* **PCS PTP Vendor State 9: Address 3.C908**

### 6.7.123 PCS PTP Vendor State 10: Address 3.C909

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Count LSW [F:0] | PTP external clock count bits 15:0 | RO | | External clock counter value |

*Table 6.7.123* **PCS PTP Vendor State 10: Address 3.C909**

### 6.7.124 PCS PTP Vendor State 11: Address 3.C90A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:0 | PTP External Clock Count MSW [1D:10] | PTP external clock count bits 29:16 | RO | | External clock counter value |

*Table 6.7.124* **PCS PTP Vendor State 11: Address 3.C90A**

### 6.7.125 PCS PTP Vendor State 12: Address 3.C90B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Seconds Count Bits 15:0 [F:0] | PTP external clock seconds count bits 15:0 | RO | | External clock seconds counter value |

*Table 6.7.125* **PCS PTP Vendor State 12: Address 3.C90B**

### 6.7.126 PCS PTP Vendor State 13: Address 3.C90C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Seconds Count Bits 31:16 [1F:10] | PTP external clock seconds count bits 31:16 | RO | | External clock seconds counter value |

*Table 6.7.126* **PCS PTP Vendor State 13: Address 3.C90C**

### 6.7.127 PCS PTP Vendor State 14: Address 3.C90D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Seconds Count Bits 47:32 [2F:20] | PTP external clock seconds count bits 47:32 | RO | | External clock seconds counter value |

*Table 6.7.127* **PCS PTP Vendor State 14: Address 3.C90D**

### 6.7.128 PCS PTP Vendor State 15: Address 3.C90E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Nanoseconds Count LSW [F:0] | PTP external clock nanoseconds count bits 15:0 | RO | | External clock nanoseconds counter value |

*Table 6.7.128* **PCS PTP Vendor State 15: Address 3.C90E**

### 6.7.129 PCS PTP Vendor State 16: Address 3.C90F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Nanoseconds Count MSW [1F:10] | PTP external clock nanoseconds count bits 31:16 | RO | | External clock nanoseconds counter value |

*Table 6.7.129* **PCS PTP Vendor State 16: Address 3.C90F**

### 6.7.130 PCS PTP Vendor State 17: Address 3.C910

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Fractional Nanoseconds Count LSW [F:0] | PTP external clock fractional nanoseconds count bits 15:0 | RO | | External clock fractional nanoseconds counter value |

*Table 6.7.130* **PCS PTP Vendor State 17: Address 3.C910**

### 6.7.131 PCS PTP Vendor State 18: Address 3.C911

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Fractional Nanoseconds Count MSW [1F:10] | PTP external clock fractional nanoseconds count bits 31:16 | RO | | External clock fractional nanoseconds counter value |

*Table 6.7.131* **PCS PTP Vendor State 18: Address 3.C911**

### 6.7.132 PCS PTP Vendor State 19: Address 3.C912

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Fractional Seconds Count LSW [F:0] | PTP external clock fractional seconds count bits 15:0 | RO | | External clock fractional seconds counter value |

*Table 6.7.132* **PCS PTP Vendor State 19: Address 3.C912**

### 6.7.133 PCS PTP Vendor State 20: Address 3.C913

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External Clock Fractional Seconds Count MSW [1F:10] | PTP external clock fractional seconds count bits 31:16 | RO | | External clock fractional seconds counter value |

*Table 6.7.133* **PCS PTP Vendor State 20: Address 3.C913**

### 6.7.134 PCS PTP Vendor State 21: Address 3.C914

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Seconds Count LSW [F:0] | PTP external GPIO clock seconds count bits 15:0 | RO | | External GPIO seconds counter value |

*Table 6.7.134* **PCS PTP Vendor State 21: Address 3.C914**

### 6.7.135 PCS PTP Vendor State 22: Address 3.C915

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Seconds Count MSW [1F:10] | PTP external GPIO clock seconds count bits 31:16 | RO | | External GPIO seconds counter value |

*Table 6.7.135* **PCS PTP Vendor State 22: Address 3.C915**

### 6.7.136 PCS PTP Vendor State 23: Address 3.C916

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Nanoseconds Count LSW [F:0] | PTP external GPIO clock nanoseconds count bits 15:0 | RO | | External GPIO nanoseconds counter value |

*Table 6.7.136* **PCS PTP Vendor State 23: Address 3.C916**

### 6.7.137 PCS PTP Vendor State 24: Address 3.C917

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Nanoseconds Count MSW [1F:10] | PTP external GPIO clock nanoseconds count bits 31:16 | RO | | External GPIO nanoseconds counter value |

*Table 6.7.137* **PCS PTP Vendor State 24: Address 3.C917**

### 6.7.138 PCS PTP Vendor State 25: Address 3.C918

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Fractional Nanoseconds Count LSW [F:0] | PTP external GPIO clock fractional nanoseconds count bits 15:0 | RO | | External GPIO fractional nanoseconds counter value |

*Table 6.7.138* **PCS PTP Vendor State 25: Address 3.C918**

### 6.7.139 PCS PTP Vendor State 26: Address 3.C919

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Fractional Nanoseconds Count MSW [1F:10] | PTP external GPIO clock fractional nanoseconds count bits 31:16 | RO | | External GPIO fractional nanoseconds counter value |

*Table 6.7.139* **PCS PTP Vendor State 26: Address 3.C919**

### 6.7.140 PCS PTP Vendor State 27: Address 3.C91A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Fractional Seconds Count LSW [F:0] | PTP external GPIO clock fractional seconds count bits 15:0 | RO | | External GPIO fractional seconds counter value |

*Table 6.7.140* **PCS PTP Vendor State 27: Address 3.C91A**

### 6.7.141 PCS PTP Vendor State 28: Address 3.C91B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP External GPIO Clock Fractional Seconds Count MSW [1F:10] | PTP external GPIO clock fractional seconds count bits 31:16 | RO | | External GPIO fractional seconds counter value |

*Table 6.7.141* **PCS PTP Vendor State 28: Address 3.C91B**

### 6.7.142 PCS PTP Vendor State 29: Address 3.C91C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PTP External GPIO Clock Update Done | PTP external GPIO clock update done | BLH | | External GPIO fractional seconds counter value |

*Table 6.7.142* **PCS PTP Vendor State 29: Address 3.C91C**

### 6.7.143 PCS PTP Egress Vendor State 1: Address 3.C930

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Egress Packet Count [2:0] | PTP Egress packet count | RO | | PTP packet count (0 to 4) |

*Table 6.7.143* **PCS PTP Egress Vendor State 1: Address 3.C930**

### 6.7.144 PCS PTP Egress Vendor State 2: Address 3.C931

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Packet Data LSW [F:0] | PTP Egress packet count | RO | | PTP packet data |

*Table 6.7.144* **PCS PTP Egress Vendor State 2: Address 3.C931**

### 6.7.145 PCS PTP Egress Vendor State 3: Address 3.C932

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Packet Data MSW [1F:10] | PTP Egress packet count | RO | | PTP packet data |

*Table 6.7.145* **PCS PTP Egress Vendor State 3: Address 3.C932**

### 6.7.146 PCS PTP Egress Vendor State 4: Address 3.C933

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PTP Egress Packet Truncated | PTP Egress packet EOP | RO | | Asserted when PTP packet has been truncated because it is longer than 128 byte. |
| 1 | PTP Egress Packet EOP | PTP Egress packet EOP | RO | | Asserted when the PTP packet data returns the last word of packet |
| 0 | PTP Egress Packet SOP | PTP Egress packet SOP | RO | | Asserted when the PTP packet data returns the first word of packet |

*Table 6.7.146* **PCS PTP Egress Vendor State 4: Address 3.C933**

### 6.7.147 PCS PTP Egress Vendor State 5: Address 3.C934

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Egress Packet Time Stamp Count [2:0] | PTP Egress packet count | RO | | PTP packet timestamp count (0 to 4) |

*Table 6.7.147* **PCS PTP Egress Vendor State 5: Address 3.C934**

### 6.7.148 PCS PTP Egress Vendor State 6: Address 3.C935

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Egress Packet Time Stamp [F:0] | PTP Egress packet count | RO | | PTP packet timestamp<br>Report arrival timestamp in 8 consecutive reads for every packet (MSB first):<br>48-bit sec, 32-bit nano-sec, 16-bit fractional nano-sec, 32-bit fractional sec |

*Table 6.7.148* **PCS PTP Egress Vendor State 6: Address 3.C935**

### 6.7.149 PCS PTP Egress Vendor State 7: Address 3.C936

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | PTP Egress RX Packet Information [6:0] | PTP Egress packet count | RO | | Received PTP packet information<br>Report diagnostic information about the type of PTP packet being received.<br>Bits[1:0]: 0=L2, 1=IPv4, 2=IPv6, 3=reserved<br>Bits[3:2]: 0=1588v1, 1=1588v2, 2=NTP/SNTP, 3=reserved<br>For IEEE 1588:<br>Bits[6:4]: 0=Sync, 1=Delay_Req, 2=General, 3=PDelay_Req, 4=Pdelay_Resp, 5=User-defined, 6 to 7=reserved<br>For NTP/SNTP:<br>Bits [6:4]: 0=Non-control, 1=Control and Private, 2 to 7=reserved |

*Table 6.7.149* **PCS PTP Egress Vendor State 7: Address 3.C936**

### 6.7.150 PCS PTP Egress Vendor State 8: Address 3.C937

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:9 | Reserved | Internal reserved - do not modify | | | |
| 8:0 | PTP USX Timestamp FIFO Count [8:0] | PTP USX timestamp FIFO count | RO | | |

*Table 6.7.150* **PCS PTP Egress Vendor State 8: Address 3.C937**

### 6.7.151 PCS PTP Egress Vendor State 9: Address 3.C938

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP USX timestamp FIFO Data 0 [F:0] | PTP USX timestamp FIFO Data 0 | RO | | |

*Table 6.7.151* **PCS PTP Egress Vendor State 9: Address 3.C938**

### 6.7.152 PCS PTP Egress Vendor State 10: Address 3.C939

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP USX timestamp FIFO Data 1 [1F:10] | PTP USX timestamp FIFO Data 1 | RO | | |

*Table 6.7.152* **PCS PTP Egress Vendor State 10: Address 3.C939**

### 6.7.153 PCS PTP Egress Vendor State 11: Address 3.C93A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP USX timestamp FIFO Data 2 [2F:20] | PTP USX timestamp FIFO Data 2 | RO | | |

*Table 6.7.153* **PCS PTP Egress Vendor State 11: Address 3.C93A**

### 6.7.154 PCS Transmit SEC Vendor Timestamp Counter 1: Address 3.C980

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Ingress Average Timestamp Counter [F:0] | SEC Ingress Average or Current Timestamp counter | RO | | When configured to perform averaging, it returns averaging value of timestamp difference between insertion and removal points. Otherwise, it returns current value of the timestamp difference. |

*Table 6.7.154* **PCS Transmit SEC Vendor Timestamp Counter 1: Address 3.C980**

### 6.7.155 PCS Transmit SEC Vendor Timestamp Counter 2: Address 3.C981

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Ingress Max Timestamp Counter [F:0] | SEC Ingress Max Timestamp counter | RO | | it returns the maximum value of timestamp difference between insertion and removal points. |

*Table 6.7.155* **PCS Transmit SEC Vendor Timestamp Counter 2: Address 3.C981**

### 6.7.156 PCS Transmit SEC Vendor Timestamp Counter 3: Address 3.C982

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Ingress Min Timestamp Counter [F:0] | SEC Ingress Min Timestamp counter | RO | | it returns the minimum value of timestamp difference between insertion and removal points. |

*Table 6.7.156* **PCS Transmit SEC Vendor Timestamp Counter 3: Address 3.C982**

### 6.7.157 PCS SEC L2 Statistics Configuration: Address 3.C9A0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:4 | SEC Ingress L2 Counter Select [3:0] | 0 = Unicast Controlled Packet<br>1 = Unicast Uncontrolled Packet<br>2 = Multicast Controlled Packet<br>3 = Multicast Uncontrolled Packet<br>4 = Broadcast Controlled Packet<br>5 = Broadcast Uncontrolled Packet<br>6 to 15 = Reserved | R/W | 0x0 | This selects the type of Ingress L2 packet counters to report (SEC Ingress L2 Counter LSW [F:0], SEC Ingress L2 Counter MSW [F:0]) |
| 3:0 | SEC Egress L2 Counter Select [3:0] | 0 = Unicast Controlled Packet<br>1 = Unicast Uncontrolled Packet<br>2 = Multicast Controlled Packet<br>3 = Multicast Uncontrolled Packet<br>4 = Broadcast Controlled Packet<br>5 = Broadcast Uncontrolled Packet<br>6 to 15 = Reserved | R/W | 0x0 | This selects the type of Egress L2 packet counters to report (SEC Egress L2 Counter LSW [F:0], SEC Egress L2 Counter MSW [F:0]) |

*Table 6.7.157* **PCS SEC L2 Statistics Configuration: Address 3.C9A0**

### 6.7.158 PCS Ingress SEC L2 Counter 1: Address 3.C9A4

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Ingress L2 Counter LSW [F:0] | SEC Ingress L2 Packet counter LSW | RO | | |

*Table 6.7.158* **PCS Ingress SEC L2 Counter 1: Address 3.C9A4**

### 6.7.159 PCS Ingress SEC L2 Counter 2: Address 3.C9A5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Ingress L2 Counter MSW [F:0] | SEC Ingress L2 Packet counter MSW | RO | | |

*Table 6.7.159* **PCS Ingress SEC L2 Counter 2: Address 3.C9A5**

### 6.7.160 PCS Egress SEC L2 Counter 1: Address 3.C9B0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Egress L2 Counter LSW [F:0] | SEC Egress L2 Packet counter LSW | RO | | |

*Table 6.7.160* **PCS Egress SEC L2 Counter 1: Address 3.C9B0**

### 6.7.161 PCS Egress SEC L2 Counter 2: Address 3.C9B1

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SEC Egress L2 Counter MSW [F:0] | SEC Egress L2 Packet counter MSW | RO | | |

*Table 6.7.161* **PCS Egress SEC L2 Counter 2: Address 3.C9B1**

### 6.7.162 PCS Transmit Vendor Alarms 1: Address 3.CC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved PCS Transmit Vendor Alarms 1 [F:4] | Reserved for future use | LH | | |
| 3 | TDE Lane Mux FIFO Parity Error | TDE Lane Mux FIFO Parity Error | LH | | |
| 2 | TDE Lane Mux FIFO Sync Error | TDE Lane Mux FIFO Sync Error | LH | | |
| 1 | XAUI Transmit Invalid 512B Block Detected | 1 = Bad 512B block detected | LH | | |
| 0 | XAUI Transmit Invalid 64B Block Detected | 1 = Bad 64B block detected | LH | | |

*Table 6.7.162* **PCS Transmit Vendor Alarms 1: Address 3.CC00**

### 6.7.163 PCS Transmit Vendor Alarms 2: Address 3.CC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved PCS Transmit Vendor Alarms 2 [F:0] | Reserved for future use | LH | | |

*Table 6.7.163* **PCS Transmit Vendor Alarms 2: Address 3.CC01**

### 6.7.164 PCS Transmit Vendor Alarms 3: Address 3.CC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved PCS Transmit Vendor Alarms 3 [F:0] | Reserved for future use | LH | | |

*Table 6.7.164* **PCS Transmit Vendor Alarms 3: Address 3.CC02**

### 6.7.165 PCS Transmit Vendor Alarms 4: Address 3.CC03

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | XFI0 Transmit Invalid XGMII Character Received | 1 = Invalid XGMII Character Received | LH | | |
| 4 | XFI0 Transmit Reserved XGMII Character Received | 1 = Reserved XGMII Character Received | LH | | |
| 3 | XFI0 Transmit 64B Encode Error | 1 = 64B Encode Error | LH | | |
| 2:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | XFI0 Transmit LOF Detected | 1 = Loss of frame detected | LH | | |

*Table 6.7.165* **PCS Transmit Vendor Alarms 4: Address 3.CC03**

### 6.7.166 PCS Standard Interrupt Mask 1: Address 3.D000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B | TX LPI Received Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | Mask for Bit 3.1.B. |
| A | RX LPI Received Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | Mask for Bit 3.1.A. |
| 9:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PCS Receive Link Status Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | Mask for Bit 3.1.2. Note this bit also shows up as Bit 3.20.C, but only as a status bit. |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.166* **PCS Standard Interrupt Mask 1: Address 3.D000**

### 6.7.167 PCS Standard Interrupt Mask 2: Address 3.D001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B | Transmit Fault Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | Bit 3.8.B |
| A | Receive Fault Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | Bit 3.8.A |
| 9:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.167* **PCS Standard Interrupt Mask 2: Address 3.D001**

### 6.7.168 PCS Standard Interrupt Mask 3: Address 3.D002

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | 10GBASE-T PCS Block Lock Latched Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | When set, this bit indicates that 10GBASE-T PCS Framer has acquired frame synchronization and is locked. This is the interrupt for bit 3.21.F |
| E | 10GBASE-T High BER Latched Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | When set, this bit indicates a high BER is being seen at the PCS. This is the interrupt for bit 3.21.E |
| D:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.168* **PCS Standard Interrupt Mask 3: Address 3.D002**

### 6.7.169 PCS Transmit Vendor Interrupt Mask 1: Address 3.D400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved PCS Transmit Vendor Alarms 1 Mask [F:4] | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0x000 | |
| 3 | TDE Lane Mux FIFO Parity Error Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |
| 2 | TDE Lane Mux FIFO Sync Error Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |

*Table 6.7.169* **PCS Transmit Vendor Interrupt Mask 1: Address 3.D400**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | XAUI Transmit Invalid 512B Block Detected Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |
| 0 | XAUI Transmit Invalid 64B Block Detected Mask | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |

*Table 6.7.169* **PCS Transmit Vendor Interrupt Mask 1: Address 3.D400** (continued)

### 6.7.170 PCS Transmit Vendor Interrupt Mask 2: Address 3.D401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved PCS Transmit Vendor Alarms 2 Mask [F:0] | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0x0000 | |

*Table 6.7.170* **PCS Transmit Vendor Interrupt Mask 2: Address 3.D401**

### 6.7.171 PCS Transmit Vendor Interrupt Mask 3: Address 3.D402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved PCS Transmit Vendor Alarms 3 Mask [F:0] | 1 = Enables interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0x000 | |

*Table 6.7.171* **PCS Transmit Vendor Interrupt Mask 3: Address 3.D402**

### 6.7.172 PCS Transmit Vendor Interrupt Mask 4: Address 3.D403

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | XFI0 Transmit Invalid XGMII Character Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 4 | XFI0 Transmit Reserved XGMII Character Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3 | XFI0 Transmit Encode 64B Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.172* **PCS Transmit Vendor Interrupt Mask 4: Address 3.D403**

### 6.7.173 PCS Transmit Vendor Debug 1: Address 3.D800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PCS TX Scrambler Disable | 1 = TX Scrambler Disabled<br>0 = Normal Operation | R/W PD | 0 | Setting this bit disables the TX scrambler during regular data transmission (for example, scrambler functionality during training and startup is unmodified). |
| E | PCS TX Inject CRC Error | 1 = Inject CRC Error | R/W | 0 | Setting this bit injects a CRC error in a single frame. |

*Table 6.7.173* **PCS Transmit Vendor Debug 1: Address 3.D800**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | PCS TX Inject Frame Error | 1 = Inject frame error | R/W | 0 | Setting this bit injects an error at the location contained in Bits C:0 in the next PCS transmission frame. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.173* **PCS Transmit Vendor Debug 1: Address 3.D800** (continued)

### 6.7.174 PCS Receive Vendor Provisioning 1: Address 3.E400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PCS RX Error LDPC Frame Enable | 1 = Enables erroring of the LDPC frame payload<br>0 = Disables erroring of the LDPC frame payload | R/W PD | 1 | Errors the entire LDPC frame payload upon an uncorrectable LDPC parity or CRC error. |

*Table 6.7.174* **PCS Receive Vendor Provisioning 1: Address 3.E400**

### 6.7.175 PCS Receive XFI0 Provisioning 1: Address 3.E460

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | XFI0 RX Descrambler Disable | 1 = XFI0 Disables PCS scrambler | R/W | 0 | PCS Descrambler Disabled. |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.175* **PCS Receive XFI0 Provisioning 1: Address 3.E460**

### 6.7.176 PCS Receive XFI0 Provisioning 2: Address 3.E461

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:9 | Reserved | Internal reserved - do not modify | | | |
| 8 | XFI0 Test Data Source | XFI0 Data pattern select<br>1 = All-zero input for pseudo-random test<br>1 = Local-fault (LF) input for pseudo-random test | R/W | 0 | Bit determines the source of the data for the pseudo-random test (selected by Bit 7). |
| 7:5 | XFI0 Test Mode Select [2:0] | Test Pattern Select:<br>xx1 = PRBS-31<br>x10 = PRBS-9<br>100 = Square-wave<br>000 = Pseudo-random | R/W | 0x0 | Note that the source for the pseudo-random test is determined by Bit 8. |
| 4 | XFI0 Test Pattern Enable | 1 = XFI0 Enables test pattern | R/W | 0 | 10GBASE-R Pseudo-Random Test Pattern Enables; see the external view for an explanation. |

*Table 6.7.176* **PCS Receive XFI0 Provisioning 2: Address 3.E461**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | XFI0 Local Fault Inject | 1 = XFI0 Injects local fault | R/W | 0 | Injects Local_Fault. |
| 2:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.176* **PCS Receive XFI0 Provisioning 2: Address 3.E461** (continued)

### 6.7.177 PCS Receive XFI1 Provisioning 1: Address 3.E470

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.177* **PCS Receive XFI1 Provisioning 1: Address 3.E470**

### 6.7.178 PCS Receive XFI1 Provisioning 2: Address 3.E471

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.178* **PCS Receive XFI1 Provisioning 2: Address 3.E471**

### 6.7.179 PCS PTP Ingress Vendor Provisioning 1: Address 3.E600

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PTP Ingress VLAN Tagging Enable | 1 = PTP Ingress VLAN tagging enabled | R/W | 0 | Enables VLAN tagging for IEEE1588 or NTP/SNTP packet (default: 0x1). |
| E | PTP Ingress IPv6/UDP Encapsulated Enabled | 1 = PTP Ingress IPv6/UDP encapsulated enabled | R/W | 0 | Enables IPv6/UDP encapsulated IEEE1588 or NTP/SNTP packet (default: 0). |
| D | PTP Ingress IPv4/UDP Encapsulated Enabled | 1 = PTP Ingress IPv4/UDP encapsulated enabled | R/W | 0 | Enables IPv4/UDP encapsulated IEEE1588 or NTP/SNTP packet (default: 0). |
| C | PTP Ingress Ethernet Encapsulated Enable | 1 = PTP Ingress Ethernet Encapsulated enabled | R/W | 0 | Enables Ethernet encapsulated IEEE1588 packet (default: 0). |
| B:A | Reserved | Internal reserved - do not modify | | | |
| 9:8 | PTP Ingress NTP Configuration [1:0] | PTP Ingress NTP/SNTP configuration | R/W | 0x0 | NTP/SNTP configuration (bit 0: 0 = client, 1 = server, bit 1: 0 = ingress, 1 = ingress). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | PTP Ingress Back Pressure Enable | 1 = PTP Ingress back pressure enabled | R/W | 0 | PTP FIFO ready enabled (default: 0):<br>Set to 1 to enable the back pressure during the appending of timestamp to the end of packet.<br>Set to 0 to disable the back pressure. |
| 4 | PTP Ingress NTP Enable | 1 = PTP Ingress NTP/SNTP enabled | R/W | 0 | Enables NTP/SNTP. |

*Table 6.7.179* **PCS PTP Ingress Vendor Provisioning 1: Address 3.E600**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | PTP Ingress 1588 Version 2 Enable | 1 = PTP Ingress 1588 version 2 enabled | R/W | 0 | Enables IEEE 1588 Version 2. |
| 0 | PTP Ingress 1588 Version 1 Enable | 1 = PTP Ingress 1588 version 1 enabled | R/W | 0 | Enables IEEE 1588 Version 1. |

*Table 6.7.179* **PCS PTP Ingress Vendor Provisioning 1: Address 3.E600** (continued)

### 6.7.180 PCS PTP Ingress Vendor Provisioning 2: Address 3.E601

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | PTP Ingress IPv6 Destination Address Matching Enable [2:0] | PTP Ingress IPv6 destination address matching enabled | R/W | 0x3 | Enables IPv6 destination address matching for IEEE1588 (default: 0x3):<br>Bit 0: FF0X:0:0:0:0:0:0:181 (X: 0x0 to 0xF)<br>Bit 1: FF02:0:0:0:0:0:0:6B<br>Bit 2: user-defined |
| B:8 | PTP Ingress IPv4 Destination Address Matching Enable [3:0] | PTP Ingress IPv4 destination address matching enabled | R/W | 0x7 | Enables IPv4 destination address matching for IEEE1588 (default: 0x7):<br>Bit 0: 224.0.1.129<br>Bit 1: 224.0.1.130-132<br>Bit 2: 224.0.0.107<br>Bit 3: user-defined |
| 7 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.180* **PCS PTP Ingress Vendor Provisioning 2: Address 3.E601**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 6:4 | PTP Ingress MAC Destination Address Matching Enable [2:0] | PTP Ingress MAC destination address matching enabled | R/W | 0x3 | Enables MAC destination address matching for IEEE1588 (default: 0x3):<br>Bit 0: 01-1B-19-00-00-00<br>Bit 1: 01-80-C2-00-00-0E<br>Bit 2: user-defined |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | PTP Ingress EtherType Matching Enable [1:0] | PTP Ingress EtherType matching enabled | R/W | 0x1 | Enables EtherType matching for Ethernet encapsulated IEEE1588 packet (default: 0x1):<br>Bit 0: 0x88F7<br>Bit 1: user-defined<br><br>This must be configured before you enable Ethernet encapsulation (at least one bit needs to be set). |

*Table 6.7.180* **PCS PTP Ingress Vendor Provisioning 2: Address 3.E601** (continued)

### 6.7.181 PCS PTP Ingress Vendor Provisioning 3: Address 3.E602

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | PTP Ingress NTP/SNTP Version [2:0] | PTP Ingress NTP/SNTP version | R/W | 0x3 | Version of NTP/SNTP (default:3); specifies the minimum value of the supported NTP/SNTP version. It must *not* be less than 3, and a value of 0 disables version checking. |
| B:8 | PTP Ingress 1588 Version [3:0] | PTP Ingress IEEE 1588 version | R/W | 0x2 | Latest version of IEEE1588 (default: 2); allows support of future versions of the IEEE 1588. It must *not* be less than 2, and a value of 0 disables version checking and assumes it is compatible with version 2. |
| 7:6 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.181* **PCS PTP Ingress Vendor Provisioning 3: Address 3.E602**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | PTP Ingress 1588 2 Step Enable | PTP Ingress 1588 2 step enabled | R/W | 0 | Set to 1 to consider two-step flag for IEEE1588v2 (or PTP_ASSIST for IEEE1588v1); this prevents timestamp overwriting for 2-step Sync message. Set to 0 to allow for timestamp update regardless of the flag (default: 0). |
| 4 | PTP Ingress 1588 Version 2 Domain Matching Enable | 1 = PTP Ingress 1588 version 2 domain matching enabled | R/W | 0 | Enables domain matching for IEEE1588v2 (default: 0). |
| 3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Ingress UDP Destination Port Matching Enable [2:0] | PTP Ingress UDP destination port matching enabled | R/W | 0x3 | Enables UDP destination port matching for IEEE 1588 or NTP/SNTP (default: 0x3):<br>Bit 0: 319 for IEEE1588, or 123 for NTP/SNTP<br>Bit 1: 320 for IEEE1588, *not* used for NTP/SNTP<br>Bit 2: user-defined |

*Table 6.7.181* **PCS PTP Ingress Vendor Provisioning 3: Address 3.E602** (continued)

### 6.7.182 PCS PTP Ingress Vendor Provisioning 4: Address 3.E603

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress EtherType [F:0] | PTP Ingress UDP destination port matching enabled | R/W | 0x0000 | User-defined EtherType for Ethernet encapsulated IEEE1588 packets (default: 0). |

*Table 6.7.182* **PCS PTP Ingress Vendor Provisioning 4: Address 3.E603**

### 6.7.183 PCS PTP Ingress Vendor Provisioning 5: Address 3.E604

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress MAC Destination Address Bits 15:0 [F:0] | PTP Ingress MAC destination address bits 15:0 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.183* **PCS PTP Ingress Vendor Provisioning 5: Address 3.E604**

### 6.7.184 PCS PTP Ingress Vendor Provisioning 6: Address 3.E605

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress MAC Destination Address Bits 31:16 [1F:10] | PTP Ingress MAC destination address bits 31:16 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.184* **PCS PTP Ingress Vendor Provisioning 6: Address 3.E605**

### 6.7.185 PCS PTP Ingress Vendor Provisioning 7: Address 3.E606

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress MAC Destination Address Bits 47:32 [2F:20] | PTP Ingress MAC destination address bits 47:32 | R/W | 0x0000 | User-defined MAC destination address (default: 0). |

*Table 6.7.185* **PCS PTP Ingress Vendor Provisioning 7: Address 3.E606**

### 6.7.186 PCS PTP Ingress Vendor Provisioning 8: Address 3.E607

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv4 Destination Address LSW [F:0] | PTP Ingress IPv4 destination address bits 15:0 | R/W | 0x0000 | User-defined IPv4 destination address (default: 0). |

*Table 6.7.186* **PCS PTP Ingress Vendor Provisioning 8: Address 3.E607**

### 6.7.187 PCS PTP Ingress Vendor Provisioning 9: Address 3.E608

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv4 Destination Address MSW [1F:10] | PTP Ingress IPv4 destination address bits 31:16 | R/W | 0x0000 | User-defined IPv4 destination address (default: 0). |

*Table 6.7.187* **PCS PTP Ingress Vendor Provisioning 9: Address 3.E608**

### 6.7.188 PCS PTP Ingress Vendor Provisioning 10: Address 3.E609

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 15:0 [F:0] | PTP Ingress IPv6 destination address bits 15:0 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.188* **PCS PTP Ingress Vendor Provisioning 10: Address 3.E609**

### 6.7.189 PCS PTP Ingress Vendor Provisioning 11: Address 3.E60A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 31:16 [1F:10] | PTP Ingress IPv6 destination address bits 31:16 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.189* **PCS PTP Ingress Vendor Provisioning 11: Address 3.E60A**

### 6.7.190 PCS PTP Ingress Vendor Provisioning 12: Address 3.E60B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 47:32 [2F:20] | PTP Ingress IPv6 destination address bits 47:32 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.190* **PCS PTP Ingress Vendor Provisioning 12: Address 3.E60B**

### 6.7.191 PCS PTP Ingress Vendor Provisioning 13: Address 3.E60C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 63:48 [3F:30] | PTP Ingress IPv6 destination address bits 63:48 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.191* **PCS PTP Ingress Vendor Provisioning 13: Address 3.E60C**

### 6.7.192 PCS PTP Ingress Vendor Provisioning 14: Address 3.E60D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 79:64 [4F:40] | PTP Ingress IPv6 destination address bits 79:64 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.192* **PCS PTP Ingress Vendor Provisioning 14: Address 3.E60D**

### 6.7.193 PCS PTP Ingress Vendor Provisioning 15: Address 3.E60E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 95:80 [5F:50] | PTP Ingress IPv6 destination address bits 95:80 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.193* **PCS PTP Ingress Vendor Provisioning 15: Address 3.E60E**

### 6.7.194 PCS PTP Ingress Vendor Provisioning 16: Address 3.E60F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 111:96 [6F:60] | PTP Ingress IPv6 destination address bits 111:96 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.194* **PCS PTP Ingress Vendor Provisioning 16: Address 3.E60F**

### 6.7.195 PCS PTP Ingress Vendor Provisioning 17: Address 3.E610

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress IPv6 Destination Address Bits 127:112 [7F:70] | PTP Ingress IPv6 destination address bits 127:112 | R/W | 0x0000 | User-defined IPv6 destination address (default: 0). |

*Table 6.7.195* **PCS PTP Ingress Vendor Provisioning 17: Address 3.E610**

### 6.7.196 PCS PTP Ingress Vendor Provisioning 18: Address 3.E611

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress UDP Destination Port [F:0] | PTP Ingress UDP destination port | R/W | 0x0000 | User-defined UDP destination port (default: 0). |

*Table 6.7.196* **PCS PTP Ingress Vendor Provisioning 18: Address 3.E611**

### 6.7.197 PCS PTP Ingress Vendor Provisioning 19: Address 3.E612

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | PTP Ingress 1588 Version 2 Domain [7:0] | PTP Ingress 1588 Version 2 Domain | R/W | 0x00 | User-defined domain for IEEE1588v2 (default: 0). |

*Table 6.7.197* **PCS PTP Ingress Vendor Provisioning 19: Address 3.E612**

### 6.7.198 PCS PTP Ingress Vendor Provisioning 20: Address 3.E613

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | PTP Ingress Correction Offset Sign | 1 = PTP Ingress correction offset sign | R/W | 0 | Correction field offset sign (0: add, 1:subtract, default: 0); indicates whether to add or subtract the correction field offset. |
| 2 | PTP Ingress Time Stamp Offset Sign | 1 = PTP Ingress time stamp offset sign | R/W | 0 | Timestamp nano-/fractional-seconds offset sign (0: add, 1:subtract, default: 0); indicates whether to add or subtract the timestamp compensation offset. |
| 1 | PTP Ingress Set Time Stamp Offset | 1 = PTP Ingress set time stamp offset | R/W | 0 | Toggle to set the new offsets of the timestamp and correction field (default: 0). |
| 0 | PTP Ingress Byte Swap | 1 = PTP Ingress byte swap | R/W | 0 | Swap byte order of the 32-bit packet data (default: 0). |

*Table 6.7.198* **PCS PTP Ingress Vendor Provisioning 20: Address 3.E613**

### 6.7.199 PCS PTP Ingress Vendor Provisioning 21: Address 3.E614

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Time Stamp Nanosecond Offset [F:0] | PTP Ingress time stamp nanosecond offset | R/W | 0x0000 | Timestamp nanoseconds offset (default: 0); compensates for the difference between MDI and timestamping point. |

*Table 6.7.199* **PCS PTP Ingress Vendor Provisioning 21: Address 3.E614**

### 6.7.200 PCS PTP Ingress Vendor Provisioning 22: Address 3.E615

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Time Stamp Fractional Second Offset LSW [F:0] | PTP Ingress time stamp fractional second offset | R/W | 0x0000 | Timestamp fractional-seconds offset (default: 0); this is the LSB 19-bit of the 32-bit fractional-seconds counter. Software checks that this value is equivalent to corresponding nanoseconds offset. |

*Table 6.7.200* **PCS PTP Ingress Vendor Provisioning 22: Address 3.E615**

### 6.7.201 PCS PTP Ingress Vendor Provisioning 23: Address 3.E616

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Ingress Time Stamp Fractional Second Offset MSW [12:10] | PTP Ingress time stamp fractional second offset | R/W | 0x0 | Timestamp fractional-seconds offset (default: 0); this is the LSB 19-bit of the 32-bit fractional-seconds counter. Software checks that this value is equivalent to the corresponding nanoseconds offset. |

*Table 6.7.201* **PCS PTP Ingress Vendor Provisioning 23: Address 3.E616**

### 6.7.202 PCS PTP Ingress Vendor Provisioning 24: Address 3.E617

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Correction Offset LSW [F:0] | PTP Ingress correction offset | R/W | 0x0000 | Correction field offset (16-bit nanosecond and 16-bit fractional nanosecond, default: 0); this compensates for the asymmetrical TX/RX delay, and/or any adjustment for transparent application. |

*Table 6.7.202* **PCS PTP Ingress Vendor Provisioning 24: Address 3.E617**

### 6.7.203 PCS PTP Ingress Vendor Provisioning 25: Address 3.E618

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Correction Offset MSW [1F:10] | PTP Ingress correction offset | R/W | 0x0000 | Correction field offset (16-bit nanosecond and 16-bit fractional nanosecond, default: 0); this compensates for the asymmetrical TX/RX delay, and/or any adjustment for transparent application. |

*Table 6.7.203* **PCS PTP Ingress Vendor Provisioning 25: Address 3.E618**

### 6.7.204 PCS PTP Ingress Vendor Provisioning 26: Address 3.E619

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B:0 | PTP Ingress Packet Action [B:0] | PTP Ingress packet action | R/W | 0x000 | IEEE 1588v2 packet action (0 = None, 1 = Capture, 2 = reserved, 3 = Capture and forward, default: 0):<br>Bits [1:0]: Sync message<br>Bits [3:2]: Delay_Req message<br>Bits [5:4]: Pdelay_Req message<br>Bits [7:6]: Pdelay_Resp message<br>Bits [9:8]: User-defined message<br>Bits [11:10]: General messages |

*Table 6.7.204* **PCS PTP Ingress Vendor Provisioning 26: Address 3.E619**

### 6.7.205 PCS PTP Ingress Vendor Provisioning 27: Address 3.E61A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:C | PTP Ingress NTP/SNTP Time Stamp Action [1:0] | PTP Ingress correct action | R/W | 0x0 | NTP/SNTP timestamp action (0 = None, 1 = Overwrite, 2 = Append, 3 = Reserved). |
| B:8 | PTP Ingress NTP/SNTP Packet Action [3:0] | PTP Ingress correct action | R/W | 0x0 | NTP/SNTP packet action (0 = None, 1 = Capture, 2 = Reserved, 3 = Capture and forward, 3 = Reserved):<br>Bits [1:0]: Non-control messages<br>Bits [3:2]: Control and Private-use messages |
| 7:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.205* **PCS PTP Ingress Vendor Provisioning 27: Address 3.E61A**

### 6.7.206 PCS PTP Ingress Vendor Provisioning 31: Address 3.E61E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PTP Ingress Packet Buffer Reset | 1 = PTP Ingress packet buffer reset | R/W | 0 | PTP packet buffer reset (default: 0).<br><br>Set to 1 to reset PTP packet extraction buffer and timestamp. |
| E:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PTP Ingress Packet Buffer Read Enable | 1 = PTP Ingress packet buffer read enabled | R/W | 0 | PTP packet buffer read (default: 0).<br><br>Toggle 0->1->0 to read the next packet data out of extraction FIFO. |

*Table 6.7.206* **PCS PTP Ingress Vendor Provisioning 31: Address 3.E61E**

### 6.7.207 PCS PTP Ingress Vendor Provisioning 32: Address 3.E61F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | PTP Ingress Packet Pause | PTP Ingress packet paused | R/W | 0 | PTP packet and timestamp extraction pause (default: 0):<br>Set to 1 to pause the extraction of packet and timestamp into the corresponding buffers.<br>Set to 0 to resume the extraction. |
| 0 | PTP Ingress Packet Size Limit | PTP Ingress packet size limited | R/W | 0 | PTP packet size limit (default: 0):<br>Set to 1 to limit PTP packet to 128-byte to ensure packet buffer is enough to fit up to 4 packets. |

*Table 6.7.207* **PCS PTP Ingress Vendor Provisioning 32: Address 3.E61F**

### 6.7.208 PCS PTP Ingress Vendor Provisioning 33: Address 3.E620

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PTP Ingress Packet Time Stamp Read Enable | 1 = PTP Ingress packet time stamp reset enabled | R/W | 0 | PTP packet timestamp read (default: 0).<br><br>Toggle 0->1->0 to read the next word of corresponding timestamp of the extracted packet. |

*Table 6.7.208* **PCS PTP Ingress Vendor Provisioning 33: Address 3.E620**

### 6.7.209 PCS PTP Ingress Vendor Provisioning 34: Address 3.E621

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B:8 | PTP Ingress 1588 Version 1 Time Stamp Action [3:0] | PTP ingress 1588 version 1 time stamp action | R/W | 0x0 | IEEE 1588v1 timestamp action (0 = None, 1 = Overwrite, 2 = Append, 3 = Remove, default: 0):<br>Bits [1:0]: Sync messages<br>Bits [3:2]: All other event messages |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | PTP Ingress 1588 Version 1 Packet Action [5:0] | PTP ingress 1588 version 1 packet action | R/W | 0x00 | IEEE 1588v1 packet action (0 = None, 1 = Capture, 2 = reserved, 3 = Capture and forward, default: 0):<br>Bits [1:0]: Sync message<br>Bits [3:2]: All other event messages<br>Bits [5:4]: General messages |

*Table 6.7.209* **PCS PTP Ingress Vendor Provisioning 34: Address 3.E621**

### 6.7.210 PCS PTP Ingress Vendor Provisioning 35: Address 3.E622

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Stacked VLAN ID [F:0] | User-defined Tag Protocol Identifier (TPID) for stacked VLAN | R/W | 0x88A8 | User-defined Tag Protocol Identifier (TPID) for stacked VLAN (default: 0x88A8 for 802.1ad). For Q-in-Q, it can be 0x9100 or another user-defined value. In addition, 0x8100 will always be recognized as valid TPID. |

*Table 6.7.210* **PCS PTP Ingress Vendor Provisioning 35: Address 3.E622**

### 6.7.211 PCS PTP Ingress Vendor Provisioning 36: Address 3.E623

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:0 | PTP Ingress Correction Action [E:0] | PTP Ingress correct action | R/W | 0x0000 | IEEE 1588v2 correction field action (default: 0):<br><br>0: No change<br>1: Correction + TS - TS(Append) + Offset<br>2: Correction + Offset<br>3: TS - Timestamp + Offset<br>(Timestamp field is set to 0 if enabled. See pif_ptp_egr_correct_clr_ts_en_i.)<br>4: Correction + TS + Offset<br>5: Correction - TS + Offset<br>6 to 7: Reserved<br><br>Bits [2:0]: Sync messages<br>Bits [5:3]: Delay_Req message<br>Bits [8:6]: Pdelay_Req message<br>Bits [11:9]: Pdelay_Resp message<br>Bits [14:12]: User-defined message |

*Table 6.7.211* **PCS PTP Ingress Vendor Provisioning 36: Address 3.E623**

### 6.7.212 PCS PTP Ingress Vendor Provisioning 37: Address 3.E624

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | PTP Ingress Time Stamp Action [9:0] | PTP Ingress packet action | R/W | 0x000 | IEEE 1588v2 timestamp action (0 = None, 1 = Overwrite, 2 = Append, 3 = Remove, default: 0):<br><br>Bits [1:0]: Sync messages<br>Bits [3:2]: Delay_Req message<br>Bits [5:4]: Pdelay_Req message<br>Bits [7:6]: Pdelay_Resp message<br>Bits [9:8]: User-defined message |

*Table 6.7.212* **PCS PTP Ingress Vendor Provisioning 37: Address 3.E624**

### 6.7.213 PCS PTP Ingress Vendor Provisioning 38: Address 3.E625

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3:0 | PTP Ingress 1588 Version 2 Message Type [3:0] | PTP Ingress 1588 version 2 message type | R/W | 0xF | IEEE 1588v2 User-defined Message Type Bit pattern to compare against messageType field after applying the bit mask (default: 0xF). |

*Table 6.7.213* **PCS PTP Ingress Vendor Provisioning 38: Address 3.E625**

### 6.7.214 PCS PTP Ingress Vendor Provisioning 39: Address 3.E626

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3:0 | PTP Ingress 1588 Version 2 Message Mask [3:0] | PTP Ingress 1588 version 2 message mask | R/W | 0xF | IEEE 1588v2 User-defined Message Mask; bit mask to compare against messageType field (for each bit, 1 = compare, 0 = ignore, default: 0xF). |

*Table 6.7.214* **PCS PTP Ingress Vendor Provisioning 39: Address 3.E626**

### 6.7.215 PCS Receive Vendor State 1: Address 3.E800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | PCS RX Current Value of Auxiliary Bit | The current value of the PCS RX auxiliary bit | RO | | This value has a maskable interrupt associated with it in 3.EC00.0. |

*Table 6.7.215* **PCS Receive Vendor State 1: Address 3.E800**

### 6.7.216 PCS Receive Reserved Vendor State 1: Address 3.E808

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Average LDPC Iteration Count [F:0] | Average LDPC iteration for 10G, 5G, or 2.5G updated every few milliseconds in 4.12 fixed point format | RO | | Obtains floating point value of LDPC iteration, by dividing value in this register by 4096. For instance, 0x1000 corresponds to Average LDPC of 1.0. |

*Table 6.7.216* **PCS Receive Reserved Vendor State 1: Address 3.E808**

### 6.7.217 PCS Receive Vendor CRC-8 Error Counter 1: Address 3.E810

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | CRC-8 Error Counter LSW [F:0] | Lower 16 bits of CRC-8 error counter | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register, and then both LSW and MSW are cleared. LSW of the counter must be read first, and MSW of counter must be read immediately after LSW is read.<br><br>A saturating counter that counts the number of uncorrectable CRC-8 or RS errors (but without LDPC frame parity error) has been detected on the received LDPC frame. |

*Table 6.7.217* **PCS Receive Vendor CRC-8 Error Counter 1: Address 3.E810**

### 6.7.218 PCS Receive Vendor CRC-8 Error Counter 2: Address 3.E811

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | CRC-8 Error Counter MSW [15:10] | Upper 6 bits of CRC-8 error counter | SCTM | 0x00 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter, and is loaded after LSW of the counter is read.<br><br>A saturating counter that counts the number of uncorrectable CRC-8 or RS errors (but without LDPC frame parity error) has been detected on the received LDPC frame. |

*Table 6.7.218* **PCS Receive Vendor CRC-8 Error Counter 2: Address 3.E811**

### 6.7.219 PCS Receive Vendor FCS No Error Frame Counter 1: Address 3.E812

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | 10GBASE-T Good Frame Counter LSW [F:0] | 10GBASE-T Good Frame Counter LSW | SCTL | 0x0000 | Counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.219* **PCS Receive Vendor FCS No Error Frame Counter 1: Address 3.E812**

### 6.7.220 PCS Receive Vendor FCS No Error Frame Counter 2: Address 3.E813

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | 10GBASE-T Good Frame Counter MSW [19:10] | 10GBASE-T Good Frame Counter MSW | SCTM | 0x000 | Counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.220* **PCS Receive Vendor FCS No Error Frame Counter 2: Address 3.E813**

### 6.7.221 PCS Receive Vendor FCS Error Frame Counter 1: Address 3.E814

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | 10GBASE-T Error Frame Counter LSW [F:0] | 10GBASE-T Bad Frame Counter LSW | SCTL | 0x0000 | Counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.221* **PCS Receive Vendor FCS Error Frame Counter 1: Address 3.E814**

### 6.7.222 PCS Receive Vendor FCS Error Frame Counter 2: Address 3.E815

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | 10GBASE-T Error Frame Counter MSW [19:10] | 10GBASE-T Bad Frame Counter MSW | SCTM | 0x000 | Counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.222* **PCS Receive Vendor FCS Error Frame Counter 2: Address 3.E815**

### 6.7.223 PCS Receive Vendor RS Corrected Error Frame Counter 1: Address 3.E816

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | RS Corrected Error Counter LSW [F:0] | Lower 16 bits of RS Corrected Frames | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter that counts the number of LDPC frames is corrected by RS code. |

*Table 6.7.223* **PCS Receive Vendor RS Corrected Error Frame Counter 1: Address 3.E816**

### 6.7.224 PCS Receive Vendor RS Corrected Error Frame Counter 2: Address 3.E817

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | RS Corrected Error Counter MSW [1F:10] | Upper 16 bits of RS Corrected Frames | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of LDPC frames and is corrected by RS code. |

*Table 6.7.224* **PCS Receive Vendor RS Corrected Error Frame Counter 2: Address 3.E817**

### 6.7.225 PCS Receive Vendor Uncorrected Frame Counter 1: Address 3.E820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Uncorrected Frame Counter LSW [F:0] | Lower 16 bits of LDPC uncorrected frames which the decoder abandoned | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of uncorrected frames. |

*Table 6.7.225* **PCS Receive Vendor Uncorrected Frame Counter 1: Address 3.E820**

### 6.7.226 PCS Receive Vendor Uncorrected Frame Counter 2: Address 3.E821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Uncorrected Frame Counter MSW [1F:10] | Upper 16 bits of LDPC uncorrected frames which the decoder abandoned | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of uncorrected frames. |

*Table 6.7.226* **PCS Receive Vendor Uncorrected Frame Counter 2: Address 3.E821**

### 6.7.227 PCS Receive RPL Vendor State 1: Address 3.E834

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:8 | Reserved | Internal reserved - do not modify | | | |
| 7:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | RPL EEE RX LPI State | 1 = RX LPI is currently detected | RO | | Indicates that RX LPI is currently detected. |
| 3 | RPL EEE RX LPI Wake Timer Fault Error | 1 = RX LPI detected a Wake Timer fault | BLH | | Indicates that RX LPI detected a Wake timer fault. |
| 2 | RPL EEE RX LPI Wake Done State | 1 = RX LPI is in Wake Done state | RO | | Indicates that RX LPI is in a Wake Done state. |
| 1 | Reserved | Internal reserved - do not modify | | | |
| 0 | RPL EEE RX LPI Active State | 1 = RX LPI is in an Active state | RO | | Indicates that RX LPI is in an Active state. |

*Table 6.7.227* **PCS Receive RPL Vendor State 1: Address 3.E834**

### 6.7.228 PCS Receive Vendor Corrected Frame 1 Iteration Counter 1: Address 3.E840

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 1 Iteration Counter LSW [F:0] | Lower 16 bits of LDPC corrected frames which converged in 1 iteration | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of corrected frames that are converged in 1 iteration. |

*Table 6.7.228* **PCS Receive Vendor Corrected Frame 1 Iteration Counter 1: Address 3.E840**

### 6.7.229 PCS Receive Vendor Corrected Frame 1 Iteration Counter 2: Address 3.E841

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 1 Iteration Counter MSW [1F:10] | Upper 16 bits of LDPC corrected frames which converged in 1 iteration | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of corrected frames that are converged in 1 iteration. |

*Table 6.7.229* **PCS Receive Vendor Corrected Frame 1 Iteration Counter 2: Address 3.E841**

### 6.7.230 PCS Receive Vendor Corrected Frame 2 Iteration Counter 1: Address 3.E842

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 2 Iteration Counter LSW [F:0] | Lower 16 bits of LDPC corrected frames which converged in 2 iterations | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of corrected frames that are converged in 2 iterations. |

*Table 6.7.230* **PCS Receive Vendor Corrected Frame 2 Iteration Counter 1: Address 3.E842**

### 6.7.231 PCS Receive Vendor Corrected Frame 2 Iteration Counter 2: Address 3.E843

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 2 Iteration Counter MSW [1F:10] | Upper 16 bits of LDPC corrected frames which converged in 2 iterations | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of corrected frames that are converged in 2 iterations. |

*Table 6.7.231* **PCS Receive Vendor Corrected Frame 2 Iteration Counter 2: Address 3.E843**

### 6.7.232 PCS Receive Vendor Corrected Frame 3 Iteration Counter 1: Address 3.E844

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 3 Iteration Counter LSW [F:0] | Lower 16 bits of LDPC corrected frames which converged in 3 iterations | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of corrected frames that are converged in 3 iterations. |

*Table 6.7.232* **PCS Receive Vendor Corrected Frame 3 Iteration Counter 1: Address 3.E844**

### 6.7.233 PCS Receive Vendor Corrected Frame 3 Iteration Counter 2: Address 3.E845

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 3 Iteration Counter MSW [1F:10] | Upper 16 bits of LDPC corrected frames which converged in 3 iterations | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of corrected frames that are converged in 3 iterations. |

*Table 6.7.233* **PCS Receive Vendor Corrected Frame 3 Iteration Counter 2: Address 3.E845**

### 6.7.234 PCS Receive Vendor Corrected Frame 4 Iteration Counter 1: Address 3.E846

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 4 Iteration Counter LSW [F:0] | Lower 16 bits of LDPC corrected frames which converged in 4 iterations | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of corrected frames that are converged in 4 iterations. |

*Table 6.7.234* **PCS Receive Vendor Corrected Frame 4 Iteration Counter 1: Address 3.E846**

### 6.7.235 PCS Receive Vendor Corrected Frame 4 Iteration Counter 2: Address 3.E847

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 4 Iteration Counter MSW [1F:10] | Upper 16 bits of LDPC corrected frames which converged in 4 iterations | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of corrected frames that are converged in 4 iterations. |

*Table 6.7.235* **PCS Receive Vendor Corrected Frame 4 Iteration Counter 2: Address 3.E847**

### 6.7.236 PCS Receive Vendor Corrected Frame 5 Iteration Counter 1: Address 3.E848

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 5 Iteration Counter LSW [F:0] | Lower 16 bits of LDPC corrected frames which converged in 5 iterations | SCTL | 0x0000 | When LSW is read, MSW is copied to a shadow register and then both LSW and MSW are cleared. LSW of the counter must be read first and MSW of the counter must be read immediately after LSW is read. A saturating counter counts the number of corrected frames that are converged in 5 iterations. |

*Table 6.7.236* **PCS Receive Vendor Corrected Frame 5 Iteration Counter 1: Address 3.E848**

### 6.7.237 PCS Receive Vendor Corrected Frame 5 Iteration Counter 2: Address 3.E849

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 5 Iteration Counter MSW [1F:10] | Upper 16 bits of LDPC corrected frames which converged in 5 iterations | SCTM | 0x0000 | MSW of the counter must be read immediately after LSW of the counter is read. MSW is actually a shadow copy of MSW of the counter and is loaded after LSW of the counter is read. A saturating counter counts the number of corrected frames that are converged in 5 iterations. |

*Table 6.7.237* **PCS Receive Vendor Corrected Frame 5 Iteration Counter 2: Address 3.E849**

### 6.7.238 PCS Receive Vendor Corrected Frame 6 Iteration Counter: Address 3.E84A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 6 Iteration Counter [F:0] | LDPC corrected frames which converged in 6 iterations | SCT | 0x0000 | Clear on read. A saturating counter counts the number of corrected frames that are converged in 6 iterations. |

*Table 6.7.238* **PCS Receive Vendor Corrected Frame 6 Iteration Counter: Address 3.E84A**

### 6.7.239 PCS Receive Vendor Corrected Frame 7 Iteration Counter: Address 3.E84B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 7 Iteration Counter [F:0] | LDPC corrected frames which converged in 7 iterations | SCT | 0x0000 | Clear on read. A saturating counter counts the number of corrected frames that are converged in 7 iterations. |

*Table 6.7.239* **PCS Receive Vendor Corrected Frame 7 Iteration Counter: Address 3.E84B**

### 6.7.240 PCS Receive Vendor Corrected Frame 8 Iteration Counter: Address 3.E84C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 8 Iteration Counter [F:0] | LDPC corrected frames which converged in 8 iterations | SCT | 0x0000 | Clear on read. A saturating counter counts the number of corrected frames that are converged in 8 iterations. |

*Table 6.7.240* **PCS Receive Vendor Corrected Frame 8 Iteration Counter: Address 3.E84C**

### 6.7.241 PCS Receive Vendor Corrected Frame 9 Iteration Counter: Address 3.E84D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 9 Iteration Counter [F:0] | LDPC corrected frames which converged in 9 iterations | SCT | 0x0000 | Clear on read. A saturating counter counts the number of corrected frames that are converged in 9 iterations. |

*Table 6.7.241* **PCS Receive Vendor Corrected Frame 9 Iteration Counter: Address 3.E84D**

### 6.7.242 PCS Receive Vendor Corrected Frame 10 Iteration Counter: Address 3.E84E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Corrected Frames 10 Iteration Counter [F:0] | LDPC corrected frames which converged in 10 iterations | SCT | 0x0000 | Clear on read. A saturating counter counts the number of corrected frames that are converged in 10 iterations. |

*Table 6.7.242* **PCS Receive Vendor Corrected Frame 10 Iteration Counter: Address 3.E84E**

### 6.7.243 PCS Receive XFI0 Vendor State 1: Address 3.E860

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI0 Good Frame Counter LSW [F:0] | XFI0 Good Frame Counter LSW | SCTL | 0x0000 | Counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.243* **PCS Receive XFI0 Vendor State 1: Address 3.E860**

### 6.7.244 PCS Receive XFI0 Vendor State 2: Address 3.E861

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI0 Good Frame Counter MSW [9:0] | XFI0 Good Frame Counter MSW | SCTM | 0x000 | Counts Ethernet good frames (for example, no Ethernet CRC-32/FCS errors). |

*Table 6.7.244* **PCS Receive XFI0 Vendor State 2: Address 3.E861**

### 6.7.245 PCS Receive XFI0 Vendor State 3: Address 3.E862

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI0 Bad Frame Counter LSW [F:0] | XFI0 Bad Frame Counter LSW | SCTL | 0x0000 | This counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.245* **PCS Receive XFI0 Vendor State 3: Address 3.E862**

### 6.7.246 PCS Receive XFI0 Vendor State 4: Address 3.E863

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | XFI0 Bad Frame Counter MSW [9:0] | XFI0 Bad Frame Counter MSW | SCTM | 0x000 | This counts Ethernet bad frames (for example, Ethernet CRC-32/FCS errors). |

*Table 6.7.246* **PCS Receive XFI0 Vendor State 4: Address 3.E863**

### 6.7.247 PCS Receive XFI0 Vendor State 5: Address 3.E864

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | XFI0 BER Counter [5:0] | XFI0 BER counter | SCT | 0x00 | 10GBASE-R BER Counter[5:0] saturating clear on read. |

*Table 6.7.247* **PCS Receive XFI0 Vendor State 5: Address 3.E864**

### 6.7.248 PCS Receive XFI0 Vendor State 6: Address 3.E865

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | XFI0 Errored Block Counter [7:0] | XFI0 errored block counter | SCT | 0x00 | 10GBASE-R Errored Block Counter[7:0] saturating clear on read. |

*Table 6.7.248* **PCS Receive XFI0 Vendor State 6: Address 3.E865**

### 6.7.249 PCS Receive XFI0 Vendor State 7: Address 3.E866

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | XFI0 Test Pattern Error Counter [F:0] | XFI0 test pattern error counter | SCT | 0x0000 | 10GBASE-R Test Pattern Error Counter[15:0] saturating clear on read. |

*Table 6.7.249* **PCS Receive XFI0 Vendor State 7: Address 3.E866**

### 6.7.250 PCS Receive XFI1 Vendor State 1: Address 3.E870

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.250* **PCS Receive XFI1 Vendor State 1: Address 3.E870**

### 6.7.251 PCS Receive XFI1 Vendor State 2: Address 3.E871

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.251* **PCS Receive XFI1 Vendor State 2: Address 3.E871**

### 6.7.252 PCS Receive XFI1 Vendor State 3: Address 3.E872

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.252* **PCS Receive XFI1 Vendor State 3: Address 3.E872**

### 6.7.253 PCS Receive XFI1 Vendor State 4: Address 3.E873

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.253* **PCS Receive XFI1 Vendor State 4: Address 3.E873**

### 6.7.254 PCS Receive XFI1 Vendor State 5: Address 3.E874

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.254* **PCS Receive XFI1 Vendor State 5: Address 3.E874**

### 6.7.255 PCS Receive XFI1 Vendor State 6: Address 3.E875

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.255* **PCS Receive XFI1 Vendor State 6: Address 3.E875**

### 6.7.256 PCS Receive XFI1 Vendor State 7: Address 3.E876

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.256* **PCS Receive XFI1 Vendor State 7: Address 3.E876**

### 6.7.257 PCS PTP Ingress Vendor State 1: Address 3.E900

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Ingress Packet Count [2:0] | PTP Ingress packet count | RO | | PTP packet count (0 to 4). |

*Table 6.7.257* **PCS PTP Ingress Vendor State 1: Address 3.E900**

### 6.7.258 PCS PTP Ingress Vendor State 2: Address 3.E901

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Packet Data LSW [F:0] | PTP Ingress packet count | RO | | PTP packet data. |

*Table 6.7.258* **PCS PTP Ingress Vendor State 2: Address 3.E901**

### 6.7.259 PCS PTP Ingress Vendor State 3: Address 3.E902

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Packet Data MSW [1F:10] | PTP Ingress packet count | RO | | PTP packet data. |

*Table 6.7.259* **PCS PTP Ingress Vendor State 3: Address 3.E902**

### 6.7.260 PCS PTP Ingress Vendor State 4: Address 3.E903

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PTP Ingress Packet Truncated | PTP Ingress packet EOP | RO | | Asserted when PTP packet has been truncated because it exceeds 128 byte length. |
| 1 | PTP Ingress Packet EOP | PTP Ingress packet EOP | RO | | Asserted when the PTP packet data returns the last word of packet. |
| 0 | PTP Ingress Packet SOP | PTP Ingress packet SOP | RO | | Asserted when the PTP packet data returns the first word of packet. |

*Table 6.7.260* **PCS PTP Ingress Vendor State 4: Address 3.E903**

### 6.7.261 PCS PTP Ingress Vendor State 5: Address 3.E904

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | PTP Ingress Packet Time Stamp Count [2:0] | PTP Ingress packet count | RO | | PTP packet timestamp count (0 to 4). |

*Table 6.7.261* **PCS PTP Ingress Vendor State 5: Address 3.E904**

### 6.7.262 PCS PTP Ingress Vendor State 6: Address 3.E905

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PTP Ingress Packet Time Stamp [F:0] | PTP Ingress packet count | RO | | PTP packet timestamp that reports arrival timestamp in 8 consecutive reads for every packet (MSB first):<br>48-bit second, 32-bit nano-second, 16-bit fractional nano-second, and 32-bit fractional second. |

*Table 6.7.262* **PCS PTP Ingress Vendor State 6: Address 3.E905**

### 6.7.263 PCS PTP Ingress Vendor State 7: Address 3.E906

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | PTP Ingress RX MAC FIFO count [7:0] | PTP Ingress RX MAC FIFO count | RO | | Read Ingress MAC RX FIFO count for determining the “base” FIFO counts (register 3:E628). |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | PTP Ingress RX Packet Information [6:0] | PTP Ingress packet count | RO | | Received PTP packet information that reports diagnostic information about the type of PTP packet being received:<br>Bits[1:0]: 0 = L2,1 = IPv4, 2 = IPv6, and 3 = Reserved.<br>Bits[3:2]: 0 = 1588v1, 1 = 1588v2, 2 = NTP/SNTP, and 3 = Reserved.<br>For IEEE 1588:<br>Bits[6:4]: 0 = Sync, 1 = Delay_Req, 2 = General, 3 = PDelay_Req, 4 = Pdelay_Resp, 5 = User-defined, and 6 to 7 = Reserved.<br>For NTP/SNTP:<br>Bits [6:4]: 0 = Non-control, 1 = Control and Private, and 2 to 7 = Reserved. |

*Table 6.7.263* **PCS PTP Ingress Vendor State 7: Address 3.E906**

### 6.7.264 PCS Receive Vendor Alarms 1: Address 3.EC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | CRC Error | 1 = RX CRC or RS Frame error | LH | | Bit is set when a CRC-8 or RS uncorrectable error is detected on the receive PCS frame. |
| E | LDPC Decode Failure | 1 = LDPC decode failure | LH | | Bit is set when the LDPC decoder fails to decode an LDPC block. |
| D | RPL Link Failure | 1 = RPL Link Failure | LH | | Bit is set when a link failure is detected in the RPL. |
| C | 40G BIP Lock | 1 = RPL 40G BIP lock | LH | | Indicates that the 40G BIP checker has achieved lock to the alignment marker. |
| B | Local Fault Detect | 1 = RPL local fault detect | LH | | Local_Fault Interrupt. |
| A | LOF Detect | 1 = RPL LOF detect | LH | | LOF Detection Interrupt. |
| 9 | Invalid 513B Block | 1 = Invalid RX 513B block received in PCS transmission frame | LH | | Bit is set when an invalid 513B block (but without an LDPC frame parity error) has been detected on the received LDPC frame. This is *only* used in enhanced DSQ128 mode. |
| 8 | Invalid 65B Block | 1 = Invalid RX 65B block received in PCS transmission frame | LH | | Bit is set when an invalid 65B block (but without an LDPC frame parity error) has been detected on the received LDPC frame. |
| 7 | EEE RX LPI Active Off | 1 = EEE RX LPI Active Off | LL | | |
| 6 | EEE RX LPI Active On | 1 = EEE RX LPI Active On | LH | | |

*Table 6.7.264* **PCS Receive Vendor Alarms 1: Address 3.EC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | LDPC Consecutive Errored Frame Exceeded | 1 = RX PCS LDPC consecutive errored frame threshold exceeded | LH | | Indicates that the consecutive LDPC errored frame has exceeded the threshold. |
| 4 | EEE RX LPI Alert | 1 = RX PCS received alert indication | LH | | Indicates that there has been an RX PCS received alert. |
| 3 | EEE RX LPI Received Latched Low | 1 = RX LPI has been detected | LL | | Indicates that an LPI ordered-set is detected. |
| 2 | EEE RX LPI Received Latched High | 1 = RX LPI has been detected | LH | | Indicates that an LPI ordered-set is detected. |
| 1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Change in Auxiliary Bit | 1 = Indicates a change in the value of the auxiliary bit | LRF | | Bit is set when a change is detected in the auxiliary bit. |

*Table 6.7.264* **PCS Receive Vendor Alarms 1: Address 3.EC00** (continued)

### 6.7.265 PCS Receive Vendor Alarms 2: Address 3.EC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.265* **PCS Receive Vendor Alarms 2: Address 3.EC01**

### 6.7.266 PCS Receive Vendor Alarms 3: Address 3.EC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.266* **PCS Receive Vendor Alarms 3: Address 3.EC02**

### 6.7.267 PCS Receive Vendor Alarms 4: Address 3.EC03

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.267* **PCS Receive Vendor Alarms 4: Address 3.EC03**

### 6.7.268 PCS Receive Vendor Alarms 5: Address 3.EC04

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | RDD Lane Mux FIFO Parity Error | RDD Lane Mux FIFO Parity Error | LH | | |
| C | RDD Lane Mux FIFO Sync Error | RDD Lane Mux FIFO Sync Error | LH | | |
| B:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.268* **PCS Receive Vendor Alarms 5: Address 3.EC04**

### 6.7.269 PCS Receive Vendor Alarms 6: Address 3.EC05

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | XFI0 Invalid 66B Character Received | 1 = XFI0 Receive invalid 66B character received | LH | | Invalid 66B code error received. |
| 2:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.269* **PCS Receive Vendor Alarms 6: Address 3.EC05**

### 6.7.270 PCS Receive Vendor Alarms 7: Address 3.EC06

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | XFI0 Receive Link Status Latch High | Status of the XFI0 receive link | LH | | Indicates the status of the XFI0 receive link. |
| 2 | Reserved | Internal reserved - do not modify | | | |
| 1 | XFI0 High BER Status | 1 = XFI0 High BER condition | LH | | |
| 0 | XFI0 Block Lock Status | 1 = XFI0 Block Lock condition | LL | | |

*Table 6.7.270* **PCS Receive Vendor Alarms 7: Address 3.EC06**

### 6.7.271 PCS Receive Vendor Alarms 10: Address 3.EC09

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | PTP Ingress Packet Gap FIFO Error | 1 = PTP Ingress packet gap FIFO error | LH | | Asserted when PTP packet gap FIFO has detected a FIFO error. |
| C | PTP Ingress Packet Gap FIFO Parity Error | 1 = PTP Ingress packet gap FIFO parity error | LH | | Asserted when PTP packet gap FIFO has detected a parity error. |
| B | PTP Ingress Packet Ready FIFO Error | 1 = PTP Ingress packet ready FIFO error | LH | | Asserted when PTP packet ready FIFO has detected a FIFO error. |
| A | PTP Ingress Packet Ready FIFO Parity Error | 1 = PTP Ingress packet ready FIFO parity error | LH | | Asserted when PTP packet ready FIFO has detected a parity error. |
| 9 | PTP Ingress Packet Remove Error | 1 = PTP Ingress packet remove error | LH | | Asserted when the packet length exceeds the UDP checksum to be updated during removal with the timestamp appended at the end of packet. When this happens, the UDP checksum is set to all-zeros. |
| 8 | PTP Ingress Packet Received | 1 = PTP Ingress packet received | LH | | Asserted when a valid PTP packet has been received, and this can be used as the valid signal for the received PTP packet information. |
| 7 | PTP Ingress Packet Pipeline FIFO Error | 1 = PTP Ingress packet pipeline FIFO error detected | LH | | Asserted when PTP packet buffer has detected a parity error. |
| 6 | PTP Ingress Packet Pipeline Parity Error | 1 = PTP Ingress packet pipeline parity error detected | LH | | Asserted when PTP timestamp buffer has detected a parity error. |

*Table 6.7.271* **PCS Receive Vendor Alarms 10: Address 3.EC09**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | PTP Ingress Time Stamp Buffer Parity Error | 1 = PTP Ingress time stamp buffer parity error detected | LH | | Asserted when PTP packet pipeline has detected a parity error. |
| 4 | PTP Ingress Packet Buffer Parity Error | 1 = PTP Ingress packet buffer parity error detected | LH | | Asserted when PTP packet pipeline has detected a FIFO error. |
| 3 | PTP Ingress Packet Correction Field Error | 1 = PTP Ingress packet correction field error | LH | | Asserted when the packet length exceeds the Correction field to be updated due to the ingress timestamp appended at the end of packet (this will *not* happen for IEEE1588v2 compliant packets). But if this happens, the Correction field will *not* be changed. |
| 2 | PTP Ingress Packet Buffer Overflow Error | 1 = PTP Ingress packet buffer overflow error detected | LH | | Asserted when PTP packet has *not* been captured because the buffer was full. |
| 1 | PTP Ingress Time Stamp Ready | 1 = PTP Ingress packet time stamp ready | RO | | Asserted when PTP packet timestamp has been captured, and it is cleared when the timestamp buffer is empty. |
| 0 | PTP Ingress Packet Ready | 1 = PTP Ingress packet ready | RO | | Asserted when PTP packet has been captured, and it is cleared when the buffer is empty. |

*Table 6.7.271* **PCS Receive Vendor Alarms 10: Address 3.EC09** (continued)

### 6.7.272 PCS Receive Vendor Interrupt Mask 1: Address 3.F400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | CRC Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit is set when a CRC-8 or RS uncorrectable error is detected on the receive PCS frame. |
| E | LDPC Decode Failure Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit is set when the LDPC decoder fails to decode an LDPC block. |
| D | RPL Link Failure Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | 40G BIP Lock Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B | Local Fault Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| A | LOF Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 9 | Invalid 513B Block Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit is set when an invalid 513B block (but without an LDPC frame parity error) has been detected on the received LDPC frame. This is only used in enhanced DSQ128 mode. |
| 8 | Invalid 65B Block Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit is set when an invalid 65B block (but without an LDPC frame parity error) has been detected on the received LDPC frame. |
| 7 | EEE RX LPI Active Off Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 6 | EEE RX LPI Active On Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.7.272* **PCS Receive Vendor Interrupt Mask 1: Address 3.F400**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | LDPC Consecutive Errored Frame Exceeded Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 4 | EEE RX LPI Alert Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3 | EEE RX LPI Received Latched Low Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2 | EEE RX LPI Received Latched High Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Change in Auxiliary Bit Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Bit is set when a change is detected in the auxiliary bit. |

*Table 6.7.272* **PCS Receive Vendor Interrupt Mask 1: Address 3.F400** (continued)

### 6.7.273 PCS Receive Vendor Interrupt Mask 2: Address 3.F401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.273* **PCS Receive Vendor Interrupt Mask 2: Address 3.F401**

### 6.7.274 PCS Receive Vendor Interrupt Mask 3: Address 3.F402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.274* **PCS Receive Vendor Interrupt Mask 3: Address 3.F402**

### 6.7.275 PCS Receive Vendor Interrupt Mask 4: Address 3.F403

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.275* **PCS Receive Vendor Interrupt Mask 4: Address 3.F403**

### 6.7.276 PCS Receive Vendor Interrupt Mask 5: Address 3.F404

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | RDD Lane Mux FIFO Parity Error | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | RDD Lane Mux FIFO Sync Error | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.276* **PCS Receive Vendor Interrupt Mask 5: Address 3.F404**

### 6.7.277 PCS Receive Vendor Interrupt Mask 6: Address 3.F405

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | XFI0 Invalid 66B Character Received Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.277* **PCS Receive Vendor Interrupt Mask 6: Address 3.F405**

### 6.7.278 PCS Receive Vendor Interrupt Mask 7: Address 3.F406

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | XFI0 Receive Link Status Latch High Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2 | Reserved | Internal reserved - do not modify | | | |
| 1 | XFI0 High BER Status Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 0 | XFI0 Block Lock Status Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.7.278* **PCS Receive Vendor Interrupt Mask 7: Address 3.F406**

### 6.7.279 PCS Receive Vendor Debug 1: Address 3.F800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PCS RX Descrambler Disable | 1 = RX Descrambler Disabled<br>0 = Normal Operation | R/W PD | 0 | Setting this bit disables the RX descrambler during regular data transmission (for example, the descrambler functionality during training and startup is unmodified). |
| E:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | PCS Network Loopback Merge | When set to 1, XAUI data from the local MAC and PCS Network Loopback data will be merged. | R/W PD | 1 | If the MAC sends data, it takes priority over the PCS Network Loopback data, and the loopback data is dropped. |
| 1 | PCS Network Loopback Pass Through | If set to 1, bit enables loopback traffic from the PCS Network Loopback to pass-through towards the System XAUI side.<br>If set to 0, data sent towards the system XUAI will be an IDLE ordered set data stream when in PCS Network Loopback. | R/W PD | 1 | Enables traffic to pass-through as well as loopback when the PCS Network Loopback is enabled. |
| 0 | PCS Network Loopback | If set to 1, data after the RX PCS layer is looped back to the TX PCS layer and transmitted back towards the network UTP line. | R/W PD | 0 | |

*Table 6.7.279* **PCS Receive Vendor Debug 1: Address 3.F800**

### 6.7.280 PCS Vendor Global Interrupt Flags 1: Address 3.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Standard Alarm 1 Interrupt | 1 = Interrupt in standard alarms 1 | RO | | An interrupt was generated from status register (see “PCS Standard Status 1: Address 3.1” on page 173) and the corresponding mask register (see “PCS Standard Interrupt Mask 1: Address 3.D000” on page 244). |
| E | Standard Alarm 2 Interrupt | 1 = Interrupt in standard alarms 2 | RO | | An interrupt was generated from status register (see “PCS Standard Status 2: Address 3.8” on page 178) and the corresponding mask register (see “PCS Standard Interrupt Mask 2: Address 3.D001” on page 244). |
| D | Standard Alarm 3 Interrupt | 1 = Interrupt in standard alarms 3 | RO | | An interrupt was generated from status register (see “PCS 10G Status 2: Address 3.21” on page 184) and the corresponding mask register (see “PCS Standard Interrupt Mask 3: Address 3.D002” on page 245). |
| C | Reserved | Internal reserved - do not modify | | | |
| B | Vendor Specific TX Alarms 1 Interrupt | 1 = Interrupt in vendor specific TX alarms 1 | RO | | An interrupt was generated from status register (see “PCS Transmit Vendor Alarms 1: Address 3.CC00” on page 242) and the corresponding mask register (see “PCS Transmit Vendor Interrupt Mask 1: Address 3.D400” on page 245). |
| A | Vendor Specific TX Alarms 2 Interrupt | 1 = Interrupt in vendor specific TX alarms 2 | RO | | An interrupt was generated from status register (see “PCS Transmit Vendor Alarms 2: Address 3.CC01” on page 242) and the corresponding mask register (see “PCS Transmit Vendor Interrupt Mask 2: Address 3.D401” on page 246). |

*Table 6.7.280* **PCS Vendor Global Interrupt Flags 1: Address 3.FC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9 | Vendor Specific TX Alarms 3 Interrupt | 1 = Interrupt in vendor specific TX alarms 3 | RO | | An interrupt was generated from status register (see “PCS Transmit Vendor Alarms 1: Address 3.CC00” on page 242) and the corresponding mask register (see “PCS Transmit Vendor Interrupt Mask 3: Address 3.D402” on page 246). |
| 8:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Vendor Specific RX Alarms 1 Interrupt | 1 = Interrupt in vendor specific RX alarms 1 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 1: Address 3.EC00” on page 288) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 1: Address 3.F400” on page 294). |
| 5 | Vendor Specific RX Alarms 2 Interrupt | 1 = Interrupt in vendor specific RX alarms 2 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 2: Address 3.EC01” on page 289) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 2: Address 3.F401” on page 295). |
| 4 | Vendor Specific RX Alarms 3 Interrupt | 1 = Interrupt in vendor specific RX alarms 3 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 3: Address 3.EC02” on page 290) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 3: Address 3.F402” on page 296). |
| 3 | Vendor Specific RX Alarms 4 Interrupt | 1 = Interrupt in vendor specific RX alarms 4 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 4: Address 3.EC03” on page 290) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 4: Address 3.F403” on page 296). |

*Table 6.7.280* **PCS Vendor Global Interrupt Flags 1: Address 3.FC00** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Vendor Specific RX Alarms 5 Interrupt | 1 = Interrupt in vendor specific RX alarms 5 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 5: Address 3.EC04” on page 290) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 5: Address 3.F404” on page 296). |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.280* **PCS Vendor Global Interrupt Flags 1: Address 3.FC00** (continued)

### 6.7.281 PCS Vendor Global Interrupt Flags 3: Address 3.FC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Vendor Specific RX Alarms 6 Interrupt | 1 = Interrupt in vendor specific RX alarms 6 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 6: Address 3.EC05” on page 291) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 6: Address 3.F405” on page 297). |
| 6 | Vendor Specific RX Alarms 7 Interrupt | 1 = Interrupt in vendor specific RX alarms 7 | RO | | An interrupt was generated from status register (see “PCS Receive Vendor Alarms 7: Address 3.EC06” on page 291) and the corresponding mask register (see “PCS Receive Vendor Interrupt Mask 7: Address 3.F406” on page 297). |
| 5:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.7.281* **PCS Vendor Global Interrupt Flags 3: Address 3.FC02**

# 6.8 PHY XS Registers

### 6.8.1 PHY XS Standard Control 1: Address 4.0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reset | 1 = PHY XS reset<br>0 = Normal operation | R/W SC | 1 | Resets the entire PHY, and the reset bit is automatically cleared upon completion of the reset sequence by the microcontroller. This bit is set to 1 during reset. The reset is internally stretched by approximately 1.7 µs. Therefore the MDIO or uP should allow for 1.7 µs before writing any PHY XS registers after this bit is set. |
| E | Loopback | 1 = System Interface Network Loopback<br>0 = Normal operation | R/W | 0 | Enables network loopback on the designated system interface.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| D | Speed Selection 0 | 1 = 10Gb/s and above<br>0 = Unspecified | ROS | 1 | This should always be set to 1 |
| C | Reserved_00a | Reserved bits 12 | R/W | 0 | |
| B | Low Power | 1 = Low-power mode<br>0 = Normal operation | R/W | 0 | A 1 written to this register causes the PHY XS to enter low-power mode. If a global chip low-power state is desired, set Bit B in "Global Standard Control 1: Address 1E.0".<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.8.1* **PHY XS Standard Control 1: Address 4.0**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A | Clock Stop Enable | 1 = The PHY XS may stop the clock during LPI<br>0 = Clock *not* stoppable | R/W | 0 | |
| 9 | XAUI Stop Enable | 1 = The PHY XS may stop XAUI signals during LPI<br>0 = XAUI *not* stoppable | R/W | 0 | |
| 8:7 | Reserved_00b [8:7] | Reserved bits [8:7] | R/W | 0x0 | |
| 6 | Speed Selection 1 | 1 = 10Gb/s and above<br>0 = Unspecified | ROS | 1 | This should always be set to 1. |
| 5:2 | Speed Selection 2 [3:0] | 1 x x x = Reserved<br>x 1 x x = Reserved<br>x x 1 x = Reserved<br>x x x 1 = Reserved<br>0 0 0 0 = 10 Gb/s | ROS | 0x0 | This should always be set to 0. |
| 1:0 | Reserved_00c [1:0] | Reserved bits [1:0] | R/W | 0x0 | |

*Table 6.8.1* **PHY XS Standard Control 1: Address 4.0** (continued)

### 6.8.2 PHY XS Standard Status 1: Address 4.1

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved_01a [F:C] | Reserved bits [15:12] | R/W | 0x0 | |
| B | TXT LPI Received | 1 = TX PHY XS has received LPI<br>0 = LPI *not* received | LH | | Source of the LPI signal is configured in 1E.C4A5.4:0. |
| A | RX LPI Received | 1 = RX PHY XS has received LPI<br>0 = LPI *not* received | LH | | Source of the LPI signal is configured in 1E.C4A4.4:0. |

*Table 6.8.2* **PHY XS Standard Status 1: Address 4.1**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9 | TX LPI Indication | 1 = TX PHY XS is currently receiving LPI<br>0 = TX PHY XS is *not* currently receiving LPI | RO | | Source of the LPI signal is configured in 1E.C4A5.4:0. |
| 8 | RX LPI Indication | 1 = RX PHY XS is currently receiving LPI<br>0 = RX PHY XS is *not* currently receiving LPI | RO | | Source of the LPI signal is configured in 1E.C4A4.4:0. |
| 7 | Fault | 1 = Fault condition detected<br>0 = No fault detected | RO | | Top-level fault indicator flag for the PHY XS (aka XAUI) block, This bit is set if either of the two bits, 4.8.B or 4.8.A, are set. |
| 6 | Clock Stop Capable | 1 = The attached PHY may stop the clock during LPI<br>0 = Clock *not* stoppable | ROS | 0 | |
| 5:3 | Reserved_01b [5:3] | Reserved bits [5:3] | R/W | 0x0 | |
| 2 | PHY XS Transmit Link Alignment Status | Status of receive XAUI interface alignment:<br><br>1 = XAUI receiver is aligned correctly<br>0 = XAUI receiver is *not* aligned | ROS | 1 | Indicates the status of the lane alignment function on the receive XAUI interface. This is a latching-low version of Bit 4.18.C. (For GEN2 PHYs, this has changed to ROS RW uP.). |
| 1 | Low Power Ability | 1 = PHY XS supports low-power mode<br>0 = No low-power mode supported | ROS | 1 | Indicates whether the XAUI interface supports a low-power mode |
| 0 | Reserved_01c | Reserved bit 0 | R/W | 0 | |

*Table 6.8.2* **PHY XS Standard Status 1: Address 4.1** (continued)

### 6.8.3 PHY XS Standard Device Identifier 1: Address 4.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.8.3* **PHY XS Standard Device Identifier 1: Address 4.2**

### 6.8.4 PHY XS Standard Device Identifier 2: Address 4.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.8.4* **PHY XS Standard Device Identifier 2: Address 4.3**

### 6.8.5 PHY XS Standard Speed Ability: Address 4.4

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved_04 [F:1] | Reserved bits [15:1] | R/W | 0x0000 | |
| 0 | 10G Capable | 1 = PHY XS is 10 Gb/s capable<br>0 = PHY XS is *not* 10 Gb/s capable | ROS | 1 | Always set to 1 in the AQR107-AQR109. |

*Table 6.8.5* **PHY XS Standard Speed Ability: Address 4.4**

### 6.8.6 PHY XS Standard Devices in Package 1: Address 4.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as there is Autonegotiation in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no DTE XAUI interface in the AQR107-AQR109. |
| 4 | PHY XS Present | 1 = PHY XS is present in package<br>0 = PHY XS is *not* present in package | ROS | 1 | Always set to 1 as there is a PHY XS interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1 as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1 as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.8.6* **PHY XS Standard Devices in Package 1: Address 4.5**

### 6.8.7 PHY XS Standard Devices in Package 2: Address 4.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the Global registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 utilizes this device for the GbE registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.7* **PHY XS Standard Devices in Package 2: Address 4.6**

### 6.8.8 PHY XS Reserved 7 Register: Address 4.7

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_07 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.8* **PHY XS Reserved 7 Register: Address 4.7**

### 6.8.9 PHY XS Standard Status 2: Address 4.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 2, as the PHY XS is present in the AQR107-AQR109. |
| D:C | Reserved_08a [D:C] | Reserved bits [13:12] | R/W | 0x0 | |
| B | Transmit Fault | 1 = Fault condition on transmit path<br>0 = No fault condition on transmit path | LH | | Bit indicates whether there is a fault somewhere along the transmit path. A fault will be indicated if there is an alignment fault, a synchronization fault on any lane, or a FIFO underflow/overflow error. |
| A | Receive Fault | 1 = Fault condition on receive path<br>0 = No fault condition on receive path | LH | | Bit indicates whether there is a fault somewhere along the receive path. A fault will be indicated if there is a FIFO underflow/overflow error. |
| 9:0 | Reserved_08b [9:0] | Reserved bits [9:0] | R/W | 0x000 | |

*Table 6.8.9* **PHY XS Standard Status 2: Address 4.8**

### 6.8.10 PHY XS Standard Package Identifier 1: Address 4.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31- 16 of Package ID | RO | | |

*Table 6.8.10* **PHY XS Standard Package Identifier 1: Address 4.E**

### 6.8.11 PHY XS Standard Package Identifier 2: Address 4.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15 - 0 of Package ID | RO | | |

*Table 6.8.11* **PHY XS Standard Package Identifier 2: Address 4.F**

### 6.8.12 PHY XS EEE Capability Register: Address 4.14

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved_14a [F:5] | Reserved bits [15:5] | R/W | 0x000 | |
| 4 | PHY XS EEE | 1 = EEE is supported for PHY XS<br>0 = EEE is *not* supported for PHY XS | ROS | 1 | |
| 3:1 | Reserved_14b [3:1] | Reserved bits [3:1] | R/W | 0x0 | |
| 0 | XAUI Stop Capable | 1 = The DTE XS may stop XAUI signals during LPI<br>0 = XAUI signals *not* stoppable | ROS | 0 | |

*Table 6.8.12* **PHY XS EEE Capability Register: Address 4.14**

### 6.8.13 PHY XS Reserved 15 Register: Address 4.15

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_15 [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.13* **PHY XS Reserved 15 Register: Address 4.15**

### 6.8.14 PHY XS EEE Wake Error Counter: Address 4.16

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | EEE Wake Error Counter [F:0] | EEE wake error counter | SCT | 0x0000 | Register is a 16-bit saturating clear on read counter. The wake error source is configured with 1E.C4A6.2:0. The default wake error source is from the TXI. |

*Table 6.8.14* **PHY XS Reserved 15 Register: Address 4.15**

### 6.8.15 PHY XS Standard XGXS Lane Status: Address 4.18

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Reserved_18a [F:D] | Reserved bits [15:13] | R/W | 0x0 | |
| C | PHY XGXS Lane Alignment Status | 1 = XAUI RX lanes aligned<br>0 = XAUI RX lanes *not* aligned | ROS | 1 | When set, bit indicates that the four XAUI RX lanes are properly aligned. This is a non-latching version of bit 4.1.2 (this includes a change to ROS RW uP to support GEN2 PHY AQrate products). |
| B | PHY XGXS Pattern Testing Ability | 1 = XAUI has the ability to generate XAUI TX test patterns<br>0 = XAUI does *not* have the ability to generate XAUI TX test patterns | ROS | 1 | Always set to 1 as the AQR107-AQR109 is capable of generating test patterns at the XAUI interface. |
| A | PHY XGXS Loopback Ability | 1 = XAUI has the ability to perform a loopback function<br>0 = XAUI does *not* have the ability to perform a loopback function | ROS | 1 | Always set to 1 as the AQR107-AQR109 is capable of performing loopback at the XAUI interface. |

*Table 6.8.15* **PHY XS Standard XGXS Lane Status: Address 4.18**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9:4 | Reserved_18b [9:4] | Reserved bits [9:4] | R/W | 0x00 | |
| 3:0 | Lane Sync [3:0] | 1 = Lane is synchronized<br>0 = Lane is *not* synchronized<br>Bit 0 corresponds to Lane 0 and so on | ROS | 0x0 | When set, these bits indicate that the corresponding lane of the XAUI interface is synchronized (this includes a change to ROS RW uP to support GEN2 PHY AQrate products). |

*Table 6.8.15* **PHY XS Standard XGXS Lane Status: Address 4.18** (continued)

### 6.8.16 PHY XS Standard XGXS Test Control: Address 4.19

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved_19a [F:3] | Reserved bits [15:3] | R/W | 0x0000 | |
| 2 | Receive Test-Pattern Enable | 1 = XAUI TX test pattern enabled<br>0 = XAUI TX test pattern *not* enabled | R/W PD | 0 | When set, bit places the transmitters of the XAUI interface into test pattern mode. |
| 1:0 | Test-Pattern Select [1:0] | 0x3 = Reserved<br>0x2 = Mixed-frequency test pattern<br>0x1 = Low-frequency test pattern<br>0x0 = High-frequency test pattern | R/W PD | 0x2 | These test patterns are described in Annex 48A of 802.3ae. These bits also interact with the Extended Test Pattern Control bits [C:B] in “PHY XS Transmit (XAUI RX) Vendor Debug 1: Address 4.D800” on page 332. The full range of options is described there, but for these functions to correspond to the test-patterns described here, bits [C:B] *must* be set to zero. |

*Table 6.8.16* **PHY XS Standard XGXS Test Control: Address 4.19**

### 6.8.17 PHY XS Reserved 1A Register: Address 4.1A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_1A [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.17* **PHY XS Reserved 1A Register: Address 4.1A**

### 6.8.18 PHY XS Reserved 1B Register: Address 4.1B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_1B [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.18* **PHY XS Reserved 1B Register: Address 4.1B**

### 6.8.19 PHY XS Reserved 1C Register: Address 4.1C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_1C [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.19* **PHY XS Reserved 1C Register: Address 4.1C**

### 6.8.20 PHY XS Reserved 1D Register: Address 4.1D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_1D [F:0] | Reserved bits [15:0] | R/W | 0x0000 | |

*Table 6.8.20* **PHY XS Reserved 1D Register: Address 4.1D**

### 6.8.21 TimeSync PHY XS Capability: Address 4.708

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | TimeSync Transmit Path Data Delay | 1 = PHY XS provides information on transmit path data delay in registers 4.1801 through 4.1804<br>0 = PHY XS does *not* provide information on transmit path data delay | RO | | |
| 0 | TimeSync Receive Path Data Delay | 1 = PHY XS provides information on receive path data delay in registers 4.1805 through 4.1808<br>0 = PHY XS does *not* provide information on receive path data delay | RO | | |

*Table 6.8.21* **TimeSync PHY XS Capability: Address 4.708**

### 6.8.22 TimeSync PHY XS Transmit Path Data Delay 1: Address 4.709

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PHY XS Transmit Path Data Delay LSW [F:0] | LSW of maximum PHY XS transmit delay in nanoseconds | RO | | |

*Table 6.8.22* **TimeSync PHY XS Transmit Path Data Delay 1: Address 4.709**

### 6.8.23 TimeSync PHY XS Transmit Path Data Delay 2: Address 4.70A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PHY XS Transmit Path Data Delay MSW [F:0] | MSW of maximum PHY XS transmit delay in nanoseconds | RO | | |

*Table 6.8.23* **TimeSync PHY XS Transmit Path Data Delay 2: Address 4.70A**

### 6.8.24 TimeSync PHY XS Transmit Path Data Delay 3: Address 4.70B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PHY XS Transmit Path Data Delay LSW [F:0] | LSW of minimum PHY XS transmit delay in nanoseconds | RO | | |

*Table 6.8.24* **TimeSync PHY XS Transmit Path Data Delay 3: Address 4.70B**

### 6.8.25 TimeSync PHY XS Transmit Path Data Delay 4: Address 4.70C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PHY XS Transmit Path Data Delay MSW [F:0] | MSW of minimum PHY XS transmit delay in nanoseconds | RO | | |

*Table 6.8.25* **TimeSync PHY XS Transmit Path Data Delay 4: Address 4.70C**

### 6.8.26 TimeSync PHY XS Receive Path Data Delay 1: Address 4.70D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PHY XS Receive Path Data Delay LSW [F:0] | LSW of maximum PHY XS receive delay in nanoseconds | RO | | |

*Table 6.8.26* **TimeSync PHY XS Receive Path Data Delay 1: Address 4.70D**

### 6.8.27 TimeSync PHY XS Receive Path Data Delay 2: Address 4.70E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Maximum PHY XS Receive Path Data Delay MSW [F:0] | MSW of maximum PHY XS receive delay in nanoseconds | RO | | |

*Table 6.8.27* **TimeSync PHY XS Receive Path Data Delay 2: Address 4.70E**

### 6.8.28 TimeSync PHY XS Receive Path Data Delay 3: Address 4.70F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PHY XS Receive Path Data Delay LSW [F:0] | LSW of minimum PHY XS receive delay in nanoseconds | RO | | |

*Table 6.8.28* **TimeSync PHY XS Receive Path Data Delay 3: Address 4.70F**

### 6.8.29 TimeSync PHY XS Receive Path Data Delay 4: Address 4.710

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Minimum PHY XS Receive Path Data Delay MSW [F:0] | MSW of minimum PHY XS receive delay in nanoseconds | RO | | |

*Table 6.8.29* **TimeSync PHY XS Receive Path Data Delay 4: Address 4.710**

### 6.8.30 PHY XS SerDes Configuration 1: Address 4.C180

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.30* **PHY XS SerDes Configuration 1: Address 4.C180**

### 6.8.31 PHY XS SerDes Lane 0 Configuration 1: Address 4.C1C0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.31* **PHY XS SerDes Lane 0 Configuration 1: Address 4.C1C0**

### 6.8.32 PHY XS SerDes Lane 1 Configuration 1: Address 4.C1D0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.32* **PHY XS SerDes Lane 1 Configuration 1: Address 4.C1D0**

### 6.8.33 PHY XS SerDes Lane 2 Configuration 1: Address 4.C1E0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.33* **PHY XS SerDes Lane 2 Configuration 1: Address 4.C1E0**

### 6.8.34 PHY XS SerDes Lane 3 Configuration 1: Address 4.C1F0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.34* **PHY XS SerDes Lane 3 Configuration 1: Address 4.C1F0**

### 6.8.35 PHY XS SerDes LUT 256: Address 4.C200

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.35* **PHY XS SerDes LUT 256: Address 4.C200**

### 6.8.36 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 1: Address 4.C440

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Reserved Transmit Provisioning C440 [2:0] | Reserved for future use | R/W PD | 0x0 | |
| C | 50MHz Primary Output Enable | This bit enables the output of the 50MHz reference clock on the primary output:<br>1 = Enables the 50MHz primary output<br>0 = Disables the 50MHz primary output | R/W PD | 0 | These fields can only be changed through the primary PHY (for example, PHY 0).<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| B | 50MHz Secondary Output Enable | This bit enables the output of the 50MHz reference clock on the secondary output:<br>1 = Enables the 50MHz secondary output<br>0 = Disables the 50MHz secondary output | R/W PD | 0 | |

*Table 6.8.36* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 1: Address 4.C440**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A:1 | Reserved Transmit Provisioning 1 [9:0] | Reserved for future use | R/W PD | 0x000 | |
| 0 | SerDes Reset | 1 = Reset SerDes<br>0 = Reset completed | R/W SC | 0 | This self-clearing register reinitializes the SerDes. If the network interface is linked, the SerDes will be reinitialized at the current line rate. If not, the rate used will be based on the SerDes startup mode.<br><br>**Note:** This bit will *not* self-clear in the absence of a valid RX signal that can be used to perform RX autocal.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.8.36* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 1: Address 4.C440** (continued)

### 6.8.37 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 2: Address 4.C441

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved Transmit Provisioning 2b [B:0] | Reserved for future use | R/W PD | 0x000 | |
| 3 | USX Autoneg Control For MAC | 1 = Enables control<br>0 = Disables control | R/W PD | 0 | USX enable/disable control for MAC. This gives USX autonegotiation control to MAC to enable/disable at any time after PHY reset. |
| 2 | Backplane ANG Enable | 1000BASE-KX or 10GBASE-KR Autoneg enable/disable bit. | R/W PD | 0 | |
| 1:0 | Reserved Transmit Provisioning 2a [1:0] | Reserved for future use | R/W PD | 0x0 | |

*Table 6.8.37* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 2: Address 4.C441**

### 6.8.38 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 3: Address 4.C442

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved Transmit Provisioning 3a [D:0] | Reserved for future use | R/W PD | 0x0000 | |
| 1 | System SGMII RX Invert | 1 = Inverts the System SGMII RX Interface | R/W PD | 0 | Inverts the SGMII RX interface (this field can *only* be changed via provisioning). |
| 0 | Reserved Transmit Provisioning 3 | Reserved for future use | R/W PD | 0 | |

*Table 6.8.38* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 3: Address 4.C442**

### 6.8.39 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 4: Address 4.C443

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved Transmit Provisioning 4a [3:0] | Reserved for future use | R/W PD | 0x0 | |
| B | System KR RX Invert | 1 = Inverts System KR RX | R/W PD | 0 | This field can *only* be changed via provisioning. |
| A:0 | Reserved Transmit Provisioning 4 [A:0] | Reserved for future use | R/W PD | 0x000 | |

*Table 6.8.39* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 4: Address 4.C443**

### 6.8.40 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 5: Address 4.C444

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Loopback Control [4:0] | 0x00 = No loopback<br>0x01 = System Interface - System Loopback<br>0x02 = Reserved<br>0x03 = System Interface - Network Loopback<br>0x04 - 0x08 = Reserved<br>0x09 = Network Interface - System Loopback<br>0x0A = Reserved<br>0x0B = Network Interface - Network Loopback<br>0x0C - 0x1F = Reserved | R/W PD | 0x00 | These bits, in conjunction with the chip configuration and the rate (Bits 1:0), select the loopback to configure for the chip. Setting one of these loopback, provisions the chip for the specified loopback. Upon clearing the loopback, the chip returns to its configuration prior to entering loopback (regardless of if any other loopbacks were selected after the initial loopback).<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| A:6 | Reserved Transmit Provisioning 5 [4:0] | Reserved for future use | R/W PD | 0x00 | |
| 5 | MDI Packet Generation | 1 = CRPAT packet generation out MDI interface<br>0 = No CRPAT packet generation out MDI interface | R/W PD | 0 | Selecting this mode of operation causes the CRPAT packet generator in the PHY to output on the MDI interface at the selected rate.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.8.40* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 5: Address 4.C444**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | Look-Aside Port Packet Generation | 1 = CRPAT packet generation out 10G look-aside interface (KR0)<br>0 = No CRPAT packet generation out 10G look-aside interface (KR0) | R/W PD | 0 | Selecting this mode of operation causes the CRPAT packet generator in the PHY to output on KR0.<br><br>**Note:** This only functions if KR1 (SERDES2) is selected as the system interface in (4.C441.F:E).<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| 3 | System I/F Packet Generation | 1 = CRPAT packet generation out 10G system interface<br>0 = No CRPAT packet generation out 10G system interface | R/W PD | 0 | Selecting this mode of operation causes the CRPAT packet generator in the PHY to output CRPAT packets on the selected 10G system interface (4.C441.F:E)<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| 2:0 | Rate [2:0] | 0x7 - 0x6 = Reserved<br>0x5 = 5G<br>0x4 = 2.5G<br>0x3 = 10G<br>0x2 = 1G<br>0x1 = 100M<br>0x0 = Reserved | R/W PD | 0x0 | These bits select the rate for the loopback and packet generation. The SerDes configuration, as well autonegotiation is controlled accordingly when a loopback is selected. For instance, if 100M system loopback on the network interface is selected, SGMII on the system interface is enabled to connect at 100M, and if passthrough is enabled 100BASE-TX will be the only advertised rate and it forces a re-autonegotiation if *not* already connected at 100M. |

*Table 6.8.40* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 5: Address 4.C444** (continued)

### 6.8.41 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 6: Address 4.C445

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Transmit Provisioning 6 [F:0] | Reserved for future use | R/W PD | 0x0000 | |

*Table 6.8.41* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 6: Address 4.C445**

### 6.8.42 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 7: Address 4.C446

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved Transmit Provisioning 7 | Reserved for future use | R/W PD | 0 | |
| E:A | KR Trng Cpost min value [E:A] | KR Trng Cpost min value | R/W PD | 0x00 | Indicates KR Trng Cpost minimum value. |
| 9:5 | KR Trng main min value [9:5] | KR Trng Cmain min value | R/W PD | 0x00 | Indicates KR Trng Cmain minimum value. |
| 4:0 | KR Trng Cpre min value [4:0] | KR Trng Cpre min value | R/W PD | 0x00 | Indicates KR Trng Cpre minimum value. |

*Table 6.8.42* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 7: Address 4.C446**

### 6.8.43 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 8: Address 4.C447

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved Transmit Provisioning 8 | Reserved for future use | R/W PD | 0 | |
| E:A | KR Trng Cpost max value [E:A] | KR Trng Cpost max value | R/W PD | 0x00 | Indicates KR Trng Cpost maximum value. |
| 9:5 | KR Trng main max value [9:5] | KR Trng Cmain max value | R/W PD | 0x00 | Indicates KR Trng Cmain maximum value. |
| 4:0 | KR Trng Cpre max value [4:0] | KR Trng Cpre max value | R/W PD | 0x00 | Indicates KR Trng Cpre maximum value. |

*Table 6.8.43* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 8: Address 4.C447**

### 6.8.44 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 9: Address 4.C448

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved Transmit Provisioning 9 | Reserved for future use | R/W PD | 0 | |
| E:A | KR Trng Cpost INIT value [E:A] | KR Trng Cpost INIT value | R/W PD | 0x00 | Indicates KR Trng Cpost INIT value. |
| 9:5 | KR Trng main INIT value [9:5] | KR Trng Cmain INIT value | R/W PD | 0x00 | Indicates KR Trng Cmain INIT value. |
| 4:0 | KR Trng Cpre INIT value [4:0] | KR Trng Cpre INIT value | R/W PD | 0x00 | Indicates KR Trng Cpre INIT value. |

*Table 6.8.44* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 9: Address 4.C448**

### 6.8.45 PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 10: Address 4.C449

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved Transmit Provisioning 10 | Reserved for future use | R/W PD | 0 | |
| E:A | KR Trng Cpost PRESET value [E:A] | KR Trng Cpost PRESET value | R/W PD | 0x00 | Indicates KR Trng Cpost PRESET value. |
| 9:5 | KR Trng main PRESET value [9:5] | KR Trng Cmain PRESET value | R/W PD | 0x00 | Indicates KR Trng Cmain PRESET value. |
| 4:0 | KR Trng Cpre PRESET value [4:0] | KR Trng Cpre PRESET value | R/W PD | 0x00 | Indicates KR Trng Cpre PRESET value. |

*Table 6.8.45* **PHY XS Transmit (XAUI RX) Reserved Vendor Provisioning 10: Address 4.C449**

### 6.8.46 PHY XS Transmit (XAUI RX) PCS Status 1: Address 4.C802

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.46* **PHY XS Transmit (XAUI RX) PCS Status 1: Address 4.C802**

### 6.8.47 PHY XS Transmit (XAUI RX) PCS Status 2: Address 4.C803

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.47* **PHY XS Transmit (XAUI RX) PCS Status 2: Address 4.C803**

### 6.8.48 PHY XS Transmit (XAUI RX) PCS Status 3: Address 4.C804

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.48* **PHY XS Transmit (XAUI RX) PCS Status 3: Address 4.C804**

### 6.8.49 PHY XS Transmit (XAUI RX) PCS Status 4: Address 4.C805

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.49* **PHY XS Transmit (XAUI RX) PCS Status 4: Address 4.C805**

### 6.8.50 PHY XS Transmit (XAUI RX) Reserved Vendor State 1: Address 4.C820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Numbers of SerDes Cals [F:0] | Number of SerDes calibrations since the last PHY reset (or power-up). | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero); this is cleared upon reset. |

*Table 6.8.50* **PHY XS Transmit (XAUI RX) Reserved Vendor State 1: Address 4.C820**

### 6.8.51 PHY XS Transmit (XAUI RX) Reserved Vendor State 2: Address 4.C821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Number of SIF Block Lock Transitions 1 - 0 [7:0] | Number of SIF block lock transitions since PHY reset from 1 to 0; for example, loss of block lock. | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero); this is cleared upon reset. |
| 7:0 | Number of SIF Block Lock Transitions 0 - 1 [7:0] | Number of SIF block lock transitions since PHY reset from 0 to 1, for example, regained block lock. | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero); this is cleared upon reset. |

*Table 6.8.51* **PHY XS Transmit (XAUI RX) Reserved Vendor State 2: Address 4.C821**

### 6.8.52 PHY XS Transmit (XAUI RX) Reserved Vendor State 3: Address 4.C822

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Number of SIF XGS Switch-overs [F:0] | Number of SIF side XGS Switch-overs since PHY Reset. | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero); this is cleared upon reset. |

*Table 6.8.52* **PHY XS Transmit (XAUI RX) Reserved Vendor State 2: Address 4.C821**

### 6.8.53 PHY XS Transmit (XAUI RX) Vendor Alarms 1: Address 4.CC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | CRPAT Test Pattern Checker Sync Error | 1 = Test pattern checker is out of sync<br>0 = Test pattern checker is in sync | LH | | |
| E:B | PRBS Test Pattern Checker Sync Error [3:0] | 1 = Test pattern checker is out of sync<br>0 = Test pattern checker is in sync | LH | | Bit 0 corresponds to lane 0 and so on. |
| A:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | OSCGMII RX FIFO Interrupt | 1 = OCSGMII RX FIFO Interrupt | LH | | |
| 0 | MACSEC Egress Interrupt | 1 = MACSEC Egress Interrupt | LH | | |

*Table 6.8.53* **PHY XS Transmit (XAUI RX) Vendor Alarms 1: Address 4.CC00**

### 6.8.54 PHY XS Transmit (XAUI RX) Vendor Alarms 2: Address 4.CC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.54* **PHY XS Transmit (XAUI RX) Vendor Alarms 2: Address 4.CC01**

### 6.8.55 PHY XS Transmit (XAUI RX) Vendor Alarms 3: Address 4.CC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Loss of Signal [3:0] | 1 = Loss of Signal on associated logical lane:<br>Bit 0: KR, SGMII<br>Bits 1 to 3: | LH | | These bits provide the Loss of Signal indication for the logical SerDes lane that loses signal. |
| B:0 | Reserved PHY XS Transmit Alarms [B:0] | Reserved | LH | | |

*Table 6.8.55* **PHY XS Transmit (XAUI RX) Vendor Alarms 3: Address 4.CC02**

### 6.8.56 PHY XS Transmit (XAUI RX) Standard Interrupt Mask 1: Address 4.D000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B | TX LPI Received Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Mask for Bit 4.1.B. |
| A | RX LPI Received Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Mask for Bit 4.1.A. |
| 9:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.56* **PHY XS Transmit (XAUI RX) Standard Interrupt Mask 1: Address 4.D000**

### 6.8.57 PHY XS Transmit (XAUI RX) Standard Interrupt Mask 2: Address 4.D001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B | Transmit Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0 | Bit 4.8.B |
| A | Receive Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0 | Bit 4.8.A |
| 9:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.57* **PHY XS Transmit (XAUI RX) Standard Interrupt Mask 2: Address 4.D001**

### 6.8.58 PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 1: Address 4.D400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | CRPAT Test Pattern Checker Sync Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0 | |
| E:B | PRBS Test Pattern Checker Sync Error Mask [3:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0x0 | |
| A:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | OCSGMI RX FIFO Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0 | |
| 0 | MACSEC Egress Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W<br>PD | 0 | |

*Table 6.8.58* **PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 1: Address 4.D400**

### 6.8.59 PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 2: Address 4.D401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.59* **PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 2: Address 4.D401**

### 6.8.60 PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 3: Address 4.D402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Loss of Signal Mask [3:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W | 0x0 | |
| B:0 | Reserved PHY XS Transmit Alarms Mask [B:0] | Reserved | R/W | 0x000 | |

*Table 6.8.60* **PHY XS Transmit (XAUI RX) Vendor Interrupt Mask 3: Address 4.D402**

### 6.8.61 PHY XS Transmit (XAUI RX) Vendor Debug 1: Address 4.D800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Test Pattern Force Error | 1 = Force test pattern error | R/W | 0 | This injects 10 PRBS Errors or 32 CRPAT errors. |
| E | Test Pattern Mode 7 Force Error | 1 = Force test pattern #7 error | R/W | 0 | This injects 32 errors. |
| D | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.61* **PHY XS Transmit (XAUI RX) Vendor Debug 1: Address 4.D800**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| C:B | Test-Pattern Extended Select [1:0] | {Test-Pattern Extended Select [C:B], Test-Pattern Select[1:0]}<br>0x0 = Annex 48A.1 High Frequency<br>0x1 = Annex 48A.2 Low Frequency<br>0x2 = Annex 48A.3 Mixed Frequency<br>0x4 = Annex 48A.4 CRPAT<br>0x5 = Annex 48A.5 CJPAT<br>0x6 = At speed CRPAT out the line<br>0x7 = PRBS-31 (x^31+x^28+1)<br>0x8 = PRBS-23 (x^23+x^18+1)<br>0x9 = PRBS-7 (x^7+x^6+1)<br>0xA = PRBS-15 (x^15+x^14+1)<br>0xF = At speed packet generator<br>0x3, 0xC -> 0xE = Reserved | R/W PD | 0x0 | These bits combine with the standard defined bits [1:0] in “PHY XS Standard XGXS Test Control: Address 4.19” on page 10 to define a broader suite of tests. |
| A | Test Pattern Check Enable | 1 = Test pattern checker enabled<br>0 = Test pattern checker *not* enabled | R/W PD | 0 | Test pattern checker enable (used for PRBS, Annex 48.4, and datapath error checking). This should *only* be enabled after you have selected the test mode. |
| 9:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Test Pattern Check Point | Test pattern check point for CRPAT and data path tests. | R/W PD | 0 | This is latched on the rising edge of "Test Pattern Check Enable" |
| 6 | Test Pattern Mode 7 Check Enable | Enable checking for Test Mode 7 | R/W PD | 0 | |

*Table 6.8.61* **PHY XS Transmit (XAUI RX) Vendor Debug 1: Address 4.D800** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | Test Pattern Invert | Inverts the PRBS generation and checking | R/W PD | 1 | Inversion can also be done using the individual TX and RX lane inversion bits. |
| 4:0 | Test Pattern Synchronization Threshold [4:0] | PRBS synchronization threshold configuration. If the number of PRBS bit errors is greater than or equal to the threshold within a 4 clock cycle window, the PRBS checker declares a synchronization error and attempt to resynchronize to the incoming PRBS pattern. Setting this to 0, disables the resynchronization. | R/W PD | 0x0A | |

*Table 6.8.61* **PHY XS Transmit (XAUI RX) Vendor Debug 1: Address 4.D800** (continued)

### 6.8.62 PHY XS Transmit (XAUI RX) Vendor Debug 2: Address 4.D801

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | Test Pattern Insert Extra Idles [2:0] | Number of extra 4 Idle Octets to insert | R/W | 0x0 | Number of extra 4 idle octets to insert in CRPAT and CJPAT generation. |
| B:8 | Test Pattern Check Select [3:0] | 1 = Enable PRBS checking on the corresponding XAUI RX Lane | R/W | 0x0 | |
| 7:4 | Reserved | Internal reserved - do not modify | | | |
| 3:0 | Test Pattern Channel Select [3:0] | 1 = Test Pattern enabled | R/W | 0x0 | Used to select which XAUI channel(s) the PRBS is inserted on. |

*Table 6.8.62* **PHY XS Transmit (XAUI RX) Vendor Debug 2: Address 4.D801**

### 6.8.63 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 1: Address 4.D810

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel 0 Test Pattern Error Counter [F:0] | A saturating 16 bit counter for errors detected from the test mode. Error counters for CRPAT, CJPAT, XAUI PRBS7,23,31 (for channel(s) selected). Note that CRPAT and CJPAT only use channel 0. | SCT | 0x0000 | Clear on read. This is a saturating 16-bit counter which accumulates the number of test errors during pattern test. Note that the API must be used to read the x^15 error counts. |

*Table 6.8.63* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 1: Address 4.D810**

### 6.8.64 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 2: Address 4.D811

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel 1 Test Pattern Error Counter [F:0] | A saturating 16 bit counter for errors detected from the test mode. Error counters for CRPAT, CJPAT, XAUI PRBS7, 23, 31 (for channel(s) selected). Note that CRPAT and CJPAT only use channel 0. | SCT | 0x0000 | Clear on read. This is a saturating 16-bit counter that accumulates the number of test errors during pattern test. Note that the API must be used to read the x^15 error counts. |

*Table 6.8.64* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 2: Address 4.D811**

### 6.8.65 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 3: Address 4.D812

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel 2 Test Pattern Error Counter [F:0] | A saturating 16 bit counter for errors detected from the test mode. Error counters for CRPAT, CJPAT, XAUI PRBS7,23,31 (for channel(s) selected). Note that CRPAT and CJPAT only use channel 0. | SCT | 0x0000 | Clear on read. This is a saturating 16-bit counter which accumulates the number of test errors during pattern test. Note that the API must be used to read the x^15 error counts. |

*Table 6.8.65* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 3: Address 4.D812**

### 6.8.66 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 4: Address 4.D813

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Channel 3 Test Pattern Error Counter [F:0] | A saturating 16 bit counter for errors detected from the test mode. Error counters for CRPAT, CJPAT, XAUI PRBS7,23,31 (for channel(s) selected). Note that CRPAT and CJPAT only use channel 0. | SCT | 0x0000 | Clear on read. This is a saturating 16-bit counter which accumulates the number of test errors during pattern test. Note that the API must be used to read the x^15 error counts. |

*Table 6.8.66* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 4: Address 4.D813**

### 6.8.67 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 5: Address 4.D814

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Test Pattern Mode 7 Error Counter [F:0] | A saturating 16 bit counter for errors detected from the test mode #7 | SCT | 0x0000 | This is a saturating 16-bit counter that accumulates the number of test errors during pattern test as specified in the test mode #7 Clause 55 test. |

*Table 6.8.67* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 5: Address 4.D814**

### 6.8.68 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 6: Address 4.D815

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet FCS Error Counter LSW [F:0] | FCS Error Counter LSW detected from the Packet Checker | SCTL | 0x0000 | This is the LSW of a saturating 32-bit counter that accumulates the number of FCS errors detected by the At-speed Packet Checker. |

*Table 6.8.68* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 6: Address 4.D815**

### 6.8.69 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 7: Address 4.D816

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet FCS Error Counter MSW [F:0] | FCS Error Counter MSW detected from the Packet Checker | SCTM | 0x0000 | This is the MSW of a saturating 32-bit counter that accumulates the number of FCS errors detected by the At-speed Packet Checker. |

*Table 6.8.69* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 7: Address 4.D816**

### 6.8.70 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 8: Address 4.D817

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet FCS No Error Counter LSW [F:0] | FCS No Error Counter LSW detected from the Packet Checker | SCTL | 0x0000 | This is the LSW of a saturating 32-bit counter that accumulates the number of packets with correct FCS detected by the At-speed Packet Checker. |

*Table 6.8.70* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 8: Address 4.D817**

### 6.8.71 PHY XS Transmit (XAUI RX) Test Pattern Error Counter 9: Address 4.D818

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet FCS No Error Counter MSW [F:0] | FCS No Error Counter MSW detected from the Packet Checker | SCTM | 0x0000 | This is the MSW of a saturating 32-bit counter that accumulates the number of packets with correct FCS detected by the At-speed Packet Checker. |

*Table 6.8.71* **PHY XS Transmit (XAUI RX) Test Pattern Error Counter 9: Address 4.D818**

### 6.8.72 PHY XS Transmit (XAUI RX) Test Pattern Error Status 1: Address 4.D820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | Packet Source Address Error | Source Address Mismatch | BLH | | . |
| 3 | Packet Destination Address Error | Destination Address Mismatch | BLH | | . |
| 2 | Packet EtherType or Length Error | EtherType or Data Length Mismatch | BLH | | . |
| 1 | Sequence Number Error | Sequence Number Mismatch | BLH | | . |
| 0 | Packet Payload Error | Payload Data Mismatch | BLH | | . |

*Table 6.8.72* **PHY XS Transmit (XAUI RX) Test Pattern Error Status 1: Address 4.D820**

### 6.8.73 PHY XS Transmit (XAUI RX) Test Pattern Error Status 2: Address 4.D821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet Payload 0 [F:0] | Payload Word 0 | RO | | The first packet payload MSW word captured after the payload mismatch. |

*Table 6.8.73* **PHY XS Transmit (XAUI RX) Test Pattern Error Status 2: Address 4.D821**

### 6.8.74 PHY XS Transmit (XAUI RX) Test Pattern Error Status 3: Address 4.D822

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet Payload 1 [F:0] | Payload Word 1 | RO | | The first packet payload LSW word captured after the payload mismatch. |

*Table 6.8.74* **PHY XS Transmit (XAUI RX) Test Pattern Error Status 3: Address 4.D822**

### 6.8.75 PHY XS Transmit (XAUI RX) Test Pattern Error Status 4: Address 4.D823

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet Payload 2 [F:0] | Payload Word 2 | RO | | The second packet payload MSW word captured after the payload mismatch. |

*Table 6.8.75* **PHY XS Transmit (XAUI RX) Test Pattern Error Status 4: Address 4.D823**

### 6.8.76 PHY XS Transmit (XAUI RX) Test Pattern Error Status 5: Address 4.D824

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Packet Payload 3 [F:0] | Payload Word 3 | RO | | The second packet payload LSW word captured after the payload mismatch. |

*Table 6.8.76* **PHY XS Transmit (XAUI RX) Test Pattern Error Status 5: Address 4.D824**

### 6.8.77 OCSGMII RX FIFO Status: Address 4.D840

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3:0 | OCSGMII RX FIFO Level [3:0] | OCSGMII RX FIFO Level | RO | | |

*Table 6.8.77* **OCSGMII RX FIFO Status: Address 4.D840**

### 6.8.78 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 1: Address 4.E410

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved Receive Provisioning 1a [D:0] | Reserved for future use | R/W PD | 0x0000 | |
| 1 | System SGMII TX Invert | 1 = Inverts System SGMII TX Interface | R/W PD | 0 | This inverts the System SGMII TX interface; this field can *only* be changed via provisioning. |
| 0 | Reserved Receive Provisioning 1 | Reserved for future use | R/W PD | 0 | |

*Table 6.8.78* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 1: Address 4.E410**

### 6.8.79 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 2: Address 4.E411

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved Receive Provisioning 2a [3:0] | Reserved for future use | R/W PD | 0x0 | |
| B | System KR TX Invert | 1 = Invert System KR TX | R/W PD | 0 | This field can *only* be changed via provisioning. |
| A | Reserved Receive Provisioning 2b | Reserved for future use | R/W PD | 0 | |
| 9 | Apply SerDes TX Settings | 1 = Apply SerDes transmit settings | R/W PD | 0 | When set to 1, the SerDes transmit settings in 4.E412 through 4.E419 are propagated to the SerDes core registers; this bit is cleared after the transfer is completed. |
| 8:0 | Reserved Receive Provisioning 2 [8:0] | Reserved for future use | R/W PD | 0x000 | |

*Table 6.8.79* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 2: Address 4.E411**

### 6.8.80 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 3: Address 4.E412

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved RX Provisioning 3 [3:0] | | R/W PD | 0x0 | |
| B:6 | SerDes Lane 0 Post Tap 1 [5:0] | | R/W PD | 0x00 | |
| 5:0 | SerDes Lane 0 Pre Tap [5:0] | | R/W PD | 0x00 | |

*Table 6.8.80* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 3: Address 4.E412**

### 6.8.81 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 4: Address 4.E413

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:9 | Reserved RX Provisioning 4 [6:0] | | R/W PD | 0x00 | |
| 8:3 | SerDes Lane 0 Main Tap [5:0] | | R/W PD | 0x00 | |
| 2:0 | SerDes Lane 0 Amplitude [2:0] | | R/W PD | 0x0 | |

*Table 6.8.81* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 4: Address 4.E413**

### 6.8.82 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 5: Address 4.E414

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 5 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.82* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 5: Address 4.E414**

### 6.8.83 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 6: Address 4.E415

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 6 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.83* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 6: Address 4.E415**

### 6.8.84 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 7: Address 4.E416

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 7 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.84* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 6: Address 4.E415**

### 6.8.85 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 8: Address 4.E417

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 8 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.85* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 8: Address 4.E417**

### 6.8.86 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 9: Address 4.E418

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 9 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.86* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 9: Address 4.E418**

### 6.8.87 PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 10: Address 4.E419

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved RX Provisioning 10 [F:0] | | R/W PD | 0x0000 | |

*Table 6.8.87* **PHY XS Receive (XAUI TX) Reserved Vendor Provisioning 10: Address 4.E419**

### 6.8.88 PIF Mailbox Extra 1: Address 4.E41D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PIF Mailbox Address Register 2 [F:0] | The data to be written, or that has been read from, the target register. | R/W PD | 0x0000 | Specifies the second target register. |

*Table 6.8.88* **PIF Mailbox Extra 1: Address 4.E41D**

### 6.8.89 PIF Mailbox Extra 2: Address 4.E41E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PIF Mailbox Data Register 2 [F:0] | The data to be written, or that has been read from, the target register. | R/W PD | 0x0000 | |

*Table 6.8.89* **PIF Mailbox Extra 2: Address 4.E41E**

### 6.8.90 PIF Mailbox Extra 3: Address 4.E41F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved RX Provisioning 16 [7:0] | Reserved for internal use | R/W PD | 0x00 | |
| 7:0 | PIF Mailbox MMD Register 2 [7:0] | MMD (upper 8 bits) specifying the second target register to read or write. | R/W PD | 0x00 | Specifies the second target register. |

*Table 6.8.90* **PIF Mailbox Extra 3: Address 4.E41F**

### 6.8.91 PHY XS Receive (XAUI TX) PCS Status 1: Address 4.E802

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.91* **PHY XS Receive (XAUI TX) PCS Status 1: Address 4.E802**

### 6.8.92 PHY XS Receive (XAUI TX) PCS Status 2: Address 4.E803

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.92* **PHY XS Receive (XAUI TX) PCS Status 2: Address 4.E803**

### 6.8.93 PHY XS Receive (XAUI TX) PCS Status 3: Address 4.E804

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.93* **PHY XS Receive (XAUI TX) PCS Status 3: Address 4.E804**

### 6.8.94 PHY XS Receive (XAUI TX) PCS Status 4: Address 4.E805

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.94* **PHY XS Receive (XAUI TX) PCS Status 4: Address 4.E805**

### 6.8.95 PHY XS Receive (XAUI TX) Reserved Vendor State 1: Address 4.E810

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Number of USX Aneg Restarts [F:0] | Number of USX autonegotiations since PHY reset. | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero). It is cleared upon reset |

*Table 6.8.95* **PHY XS Receive (XAUI TX) Reserved Vendor State 1: Address 4.E810**

### 6.8.96 PHY XS System Interface Connection Status: Address 4.E812

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | System Interface Autoneg Status [1:0] | 0 = N/A<br>1 = Not Complete<br>2 = Complete<br>3 = Reserved | RO | | Indicates the completion progress of the system interface's autonegotiation. |
| D | RX Link Up | 0 = Link Not Up<br>1 = Link Up | RO | | Indicates that the system interface has linked and is ready to receive. |
| C | TX Ready | 0 = Not Ready<br>1 = Ready | RO | | Indicates that the system interface is ready to transmit. |
| B:8 | System Interface Rate [3:0] | 0 = Low Power<br>1 = 100M<br>2 = 1G<br>3 = 10G<br>4 = 2.5G<br>5 = 5G<br>6 - 0xF = Reserved | RO | | Indicates the currently active data rate for the system interface. |

*Table 6.8.96* **PHY XS System Interface Connection Status: Address 4.E812**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7:3 | System Interface In Use [4:0] | 0 = Backplane KR<br>1 = Backplane KX<br>2 = XFI<br>3 = USXGMII<br>4 = XAUI<br>5 = XAUI Pause Based<br>6 = SGMII<br>7 = RXAUI<br>8 = MAC<br>9 = OFF<br>0xA = OCSGMII<br>0xB = Unknown<br>0xC - 0x1F = Reserved | RO | | Indicates the currently active mode for the system interface. |
| 2:0 | Reserved Receive State 3 [2:0] | Reserved for future use | RO | | |

*Table 6.8.96* **PHY XS System Interface Connection Status: Address 4.E812** (continued)

### 6.8.97 PHY XS Receive (XAUI TX) Vendor Alarms 1: Address 4.EC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | MACSEC Ingress Interrupt | 1 = MACSEC Ingress Interrupt | LH | | |

*Table 6.8.97* **PHY XS Receive (XAUI TX) Vendor Alarms 1: Address 4.EC00**

### 6.8.98 PHY XS Receive (XAUI TX) Vendor Alarms 2: Address 4.EC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | System Interface RX Link Up | 1 = System Interface RX has come up | LH | | Bit indicates that the SerDes receive link has come up. This is an alarm bit that corresponds to a 1 value of the status bit: 4.E812.D |
| E | System Interface RX Link Down | 1 = System Interface RX has gone down | LH | | Bit indicates that the SerDes receive link has gone down. This is an alarm bit that corresponds to a 0 value of the status bit: 4.E812.D |
| D | System Interface TX Ready | 1 = System Interface TX has become ready to transmit | LH | | Bit indicates that the SerDes transmit link has become ready to transmit. This is an alarm bit that corresponds to a 1 value of the status bit: 4.E812.C |
| C | System Interface TX Not Ready | 1 = System Interface TX has become *not* -ready to transmit | LH | | Bit indicates that the SerDes transmit link has become *not* -ready to transmit. This is an alarm bit that corresponds to a 0 value of the status bit: 4.E812.C |
| B:0 | Reserved PHY XS Receive Alarms 2 [B:0] | Reserved | LH | | |

*Table 6.8.98* **PHY XS Receive (XAUI TX) Vendor Alarms 2: Address 4.EC01**

### 6.8.99 PHY XS Receive (XAUI TX) Vendor Interrupt Mask 1: Address 4.F400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | MACSEC Ingress Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.8.99* **PHY XS Receive (XAUI TX) Vendor Interrupt Mask 1: Address 4.F400**

### 6.8.100 PHY XS Receive (XAUI TX) Vendor Interrupt Mask 2: Address 4.F401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | System Interface RX Link Up Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Setting this bit to 1 enables interrupt generation.<br>Setting this bit to 0 disables interrupt generation.<br><br>Mask for alarm: 4.EC01.F |
| E | System Interface RX Link Down Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Setting this bit to 1 enables interrupt generation.<br>Setting this bit to 0 disables interrupt generation.<br><br>Mask for alarm: 4.EC01.E |
| D:0 | Reserved PHY XS Receive Alarms 2 Mask [D:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0x0000 | Setting this bit to 1 enables interrupt generation.<br>Setting this bit to 0 disables interrupt generation. |

*Table 6.8.100* **PHY XS Receive (XAUI TX) Vendor Interrupt Mask 2: Address 4.F401**

### 6.8.101 PHY XS Receive (XAUI TX) Vendor Debug 1: Address 4.F800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.101* **PHY XS Receive (XAUI TX) Vendor Debug 1: Address 4.F800**

### 6.8.102 PHY XS Receive (XAUI TX) Vendor Debug 2: Address 4.F801

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.102* **PHY XS Receive (XAUI TX) Vendor Debug 2: Address 4.F801**

### 6.8.103 PHY XS Receive (XAUI TX) Vendor Debug 3: Address 4.F802

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.103* **PHY XS Receive (XAUI TX) Vendor Debug 3: Address 4.F802**

### 6.8.104 PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Standard Alarms 1 Interrupt | 1 = Interrupt in standard alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| E | Standard Alarms 2 Interrupt | 1 = Interrupt in standard alarms 2 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| D:B | Reserved | Internal reserved - do not modify | | | |
| A | Vendor Specific TX Alarms 1 Interrupt | 1 = Interrupt in vendor specific TX alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 9 | Reserved | Internal reserved - do not modify | | | |
| 8 | Vendor Specific TX Alarms 3 Interrupt | 1 = Interrupt in vendor specific TX alarms 3 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 7:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | Vendor Specific RX Alarms 1 Interrupt | 1 = Interrupt in vendor specific RX alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 1 | Vendor Specific RX Alarms 2 Interrupt | 1 = Interrupt in vendor specific RX alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.8.104* **PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00**

# 6.9 Autonegotiation Registers

### 6.9.1 Autonegotiation Standard Control 1: Address 7.0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reset | 1 = Autonegotiation reset<br>0 = Normal operation | R/W SC | 1 | Resets the entire PHY. The reset bit is automatically cleared after the reset sequence by the microcontroller completes. This bit is set to 1 during reset. The reset is internally stretched by approximately 1.7 µs.<br><br>Therefore, the MDIO or uP should allow for 1.7 µs before writing any Autonegotiation registers after this bit is set. |
| E | Reserved_0a | Reserved bit 14 | R/W PD | 0 | |
| D | Extended Next Page Control | 1 = Enables Extended Next Pages<br>0 = Disables Extended Next Pages | R/WP D | 1 | This bit is OR'ed with bit 7.10.C. |
| C | Autonegotiation Enable | 1 = Enables autonegotiation<br>0 = Disables autonegotiation | R/W PD | 1 | When enabled, autonegotiation determines the link speed. If this bit is disabled, autonegotiation is disabled. |
| B:A | Reserved_0b [B:A] | Reserved bits 11 to 10 | R/W PD | 0x0 | |
| 9 | Restart Autonegotiation | 1 = Restart autonegotiation process<br>0 = Normal operation | R/W SC | 0 | **Note:** This is a processor-intensive operation. 1E.C831.F. Completion of this operation can be monitored via 1E.C831.F. |
| 8:0 | Reserved_0c [8:0] | Reserved bits 8 to 0 | R/W PD | 0x000 | |

*Table 6.9.1* **Autonegotiation Standard Control 1: Address 7.0**

### 6.9.2 Autonegotiation Standard Status 1: Address 7.1

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved_1a [F:A] | Reserved bits 15 to 10 | R/W | 0x00 | |
| 9 | Parallel Detection Fault | 1 = A fault has been detected via the parallel detection function<br>0 = No fault has been detected via the parallel detection function | LH | | |
| 8 | Reserved_1b | Reserved bit 8 | R/W | 0 | |
| 7 | Extended Next Page Status | 1 = Extended Next Page is used<br>0 = Extended Next Page is *not* used | RO | | Indicates that both the local device and the link partner have indicated support for the Extended Next Page. |
| 6 | Page Received | 1 = A page has been received<br>0 = A page has *not* been received | LH | | Indicates that a page has been received. If it is a regular page, it is placed in 7.13 ->7.15. If it is an Extended Next Page, it is placed in registers 7.19 -> 7.1B. |
| 5 | Autonegotiation Complete | 1 = Autonegotiation has completed<br>0 = Autonegotiation is in process | RO | | Indicates the Autonegotiation receive link status. |
| 4 | Remote Fault | 1 = Remote Fault condition has been detected<br>0 = No Remote Fault condition has been detected | LH | | Indicates that the remote PHY has a fault. |
| 3 | Autonegotiation Ability | 1 = PHY is able to perform autonegotiation<br>0 = PHY is *not* able to perform autonegotiation | ROS | 1 | Always set as 1 as the local device has autonegotiation ability. |

*Table 6.9.2* **Autonegotiation Standard Status 1: Address 7.1**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Link Status | 1 = Link is currently up<br>0 = Link has been lost since last read | LL | | This bit it is a duplicate of the PMA link status bit in 1.1.2. Note that this is latching low, so it can *only* be used to detect link drops, and it does *not* indicate the current status of the link without performing back-to-back reads. |
| 1 | Reserved_1c | Reserved bit 1 | R/W | 0 | |
| 0 | Link Partner Autonegotiation Ability | 1 = Link Partner is able to perform autonegotiation<br>0 = Link Partner is *not* able to perform autonegotiation | RO | | |

*Table 6.9.2* **Autonegotiation Standard Status 1: Address 7.1** (continued)

### 6.9.3 Autonegotiation Standard Device Identifier 1: Address 7.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.9.3* **Autonegotiation Standard Device Identifier 1: Address 7.2**

### 6.9.4 Autonegotiation Standard Device Identifier 2: Address 7.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.9.4* **Autonegotiation Standard Device Identifier 2: Address 7.3**

### 6.9.5 Autonegotiation Standard Devices in Package 1: Address 7.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as there is Autonegotiation in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no DTE XAUI interface in the AQR107-AQR109. |
| 4 | PHY XS Present | 1 = PHY XS is present in package<br>0 = PHY XS is *not* present in package | ROS | 1 | Always set to 1, as there is a PHY XS interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1, as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1, as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.9.5* **Autonegotiation Standard Devices in Package 1: Address 7.5**

### 6.9.6 Autonegotiation Standard Devices in Package 2: Address 7.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the global control registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the GbE registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.6* **Autonegotiation Standard Devices in Package 2: Address 7.6**

### 6.9.7 Autonegotiation Standard Status 2: Address 7.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 0x2, as the Autonegotiation resides here in the AQR107-AQR109. |
| D:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.7* **Autonegotiation Standard Status 2: Address 7.8**

### 6.9.8 Autonegotiation Standard Package Identifier 1: Address 7.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31- 16 of Package ID | RO | | |

*Table 6.9.8* **Autonegotiation Standard Package Identifier 1: Address 7.E**

### 6.9.9 Autonegotiation Standard Package Identifier 2: Address 7.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15 - 0 of Package ID | RO | | |

*Table 6.9.9* **Autonegotiation Standard Package Identifier 2: Address 7.F**

### 6.9.10 Autonegotiation Advertisement Register: Address 7.10†

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Next Page Ability | 1 = Next Page ability | R/W PD | 1 | If a device implements Next Page ability and wishes to engage in Next Page exchange, it needs to set the NP bit to 1. Note that a device may implement Next Page ability and choose *not* to engage in Next Page exchange by setting the NP bit to a 0. |
| E | Reserved_7a | Reserved bit 14 | R/W PD | 0 | |

*Table 6.9.10* **Autonegotiation Advertisement Register: Address 7.10**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Advertisement Remote Fault | 1 = Remote Fault | R/W | 0 | The Remote Fault (RF) bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1, the RF bit is set to 1.<br><br>**Note:** The PHY does *not* support a Remote Fault sensing function. |
| C | Extended Next Page Ability | 1 = Extended Next Page capable<br>0 = Not capable of Extended Next Pages | R/W PD | 1 | The Extended Next Page (XNP) bit indicates the local device support status: it supports transmission of Extended Next Pages when set to 1, and the local device does *not* support Extended Next Pages when set to 0. |

*Table 6.9.10* **Autonegotiation Advertisement Register: Address 7.10** (continued)



† This register is used in conjunction with bit 7.C400.5 to hard provision the autonegotiation base page that will be sent.

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| B:5 | Technology Ability Field [6:0] | Bit 0: 10BASE-T<br>Bit 1: 10BASE-T full duplex<br>Bit 2: 100BASE-TX<br>Bit 3: 100BASE-TX full duplex<br>Bit 4: 100BASE-T4<br>Bit 5: PAUSE operation for full duplex links<br>Bit 6: Asymmetric PAUSE operation for full duplex links | R/W PD | 0x00 | The Technology Ability Field contains information that indicates the supported technologies defined in Annex 28B.2 and Annex 28D. Multiple technologies may be advertised in the link code word. A device supports the data service ability for any technology that it advertises.<br><br>Since the PHY does *not* support 10BASE-T or 100BASE-T4, these bits (0, 1, 4) should always be set to zero. |
| 4:0 | Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | R/W PD | 0x01 | Field should always be set to 0x01 as the PHY is only capable of handling 802.3 Ethernet. |

*Table 6.9.10* **Autonegotiation Advertisement Register: Address 7.10** (continued)

### 6.9.11 Autonegotiation Link Partner Base Page Ability Register: Address 7.13

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner Next Page Ability | 1 = Next Page ability<br>0 = Next Page ability *not* supported or *not* engaged | RO | | If Next Page ability is *not* supported, the Next Page (NP) bit is always set to 0. If a device implements Next Page ability and wishes to engage in Next Page exchange, it *must* set the NP bit to logic 1. |
| E | Link Partner Base Page Acknowledge | 1 = Acknowledge | RO | | An Acknowledge (ACK) is used by the Autonegotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. |

*Table 6.9.11* **Autonegotiation Link Partner Base Page Ability Register: Address 7.13**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Link Partner Remote Fault | 1 = Remote Fault | RO | | The Remote Fault (RF) bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1, the RF bit is set to 1. |
| C | Link Partner Extended Next Page Ability | 1 = Extended Next Page capable<br>0 = Not capable of Extended Next Pages | RO | | The Extended Next Page indicates that the link partner has indicated support for the Extended Next Page when set to 1. When set to 0, the link partner does *not* support Extended Next Page. |
| B:5 | Link Partner Technology Ability Field [6:0] | Bit 0: 10BASE-T<br>Bit 1: 10BASE-T full duplex<br>Bit 2: 100BASE-TX<br>Bit 3: 100BASE-TX full duplex<br>Bit 4: 100BASE-T4<br>Bit 5: PAUSE operation for full duplex links<br>Bit 6: Asymmetric PAUSE operation for full duplex links | RO | | Technology ability field contains information indicating supported technologies defined in Annex 28B.2 and Annex 28D. Multiple technologies may be advertised in the link code word. A device shall support the data service ability for a technology it advertises. The arbitration function determines the common mode of operation shared by a link partner and resolves the multiple common modes. |
| 4:0 | Link Partner Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | RO | | Selector field encodes 32 possible messages defined in Annex 28A. Combinations *not* specified are reserved for future use and shall *not* be transmitted. |

*Table 6.9.11* **Autonegotiation Link Partner Base Page Ability Register: Address 7.13** (continued)

### 6.9.12 Autonegotiation Extended Next Page Transmit Register: Address 7.16†

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Next Page | 1 = Additional Next Page follows<br>0 = Last page | R/W | 0 | Next Page is used by the Next Page function to indicate whether or *not* this is the last Next Page to be transmitted. |
| E | Reserved_16a | Reserved bit 14 | R/W | 0 | |
| D | Message Page | 1 = Message Page<br>0 = Unformatted page | R/W | 0 | Message Page is used by the Next Page function to differentiate a Message Page from an unformatted page. |
| C | Acknowledge 2 | 1 = Comply with corresponding message<br>0 = Cannot comply with corresponding message | R/W | 0 | Acknowledge 2 is used by the Next Page function to indicate that a device has the ability to comply with the message. |
| B | Toggle | Value of toggle bit | RO | | Set to opposite of the corresponding bit in the previous page. |
| A:0 | Message Code Field [A:0] | [A:0] = Message Code Field:<br><br>0x0 = Reserved<br>0x1 = Null message<br>0x2 -> 0x3 Reserved Expansion message<br>0x4 = Remote Fault details message<br>0x5 = OUI message<br>0x6 = PHY ID message<br>0x7 = 100BASE-T2 message<br>0x8 = 1000BASE-T message<br>0x9 = 10GBASE-T message | R/W PD | 0x001 | Interpreted as message code (see 802.3 Appendix 28C) if Message Page bit is set to one (7.16:1). Otherwise interpreted as an unformatted code field. |

*Table 6.9.12* **Autonegotiation Extended Next Page Transmit Register: Address 7.16**

† This register is used in conjunction with bit 7.C400.5 and registers 7.17 and 7.18 to hard provision the autonegotiation Extended Next Page that will be sent. Using this it is possible to hard-code the 1G and 10G capabilities, as well as short-reach capability.

### 6.9.13 Autonegotiation Extended Next Page Unformatted Code Register 1: Address 7.17

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Unformatted Code Field 1 [1F:10] | [F:0] = Unformatted Code Field 1 | R/W PD | 0x0000 | |

*Table 6.9.13* **Autonegotiation Extended Next Page Unformatted Code Register 1: Address 7.17**

### 6.9.14 Autonegotiation Extended Next Page Unformatted Code Register 2: Address 7.18

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Unformatted Code Field 2 [2F:20] | [F:0] = Unformatted Code Field 2 | R/W PD | 0x0000 | |

*Table 6.9.14* **Autonegotiation Extended Next Page Unformatted Code Register 2: Address 7.18**

### 6.9.15 Autonegotiation Link Partner Extended Next Page Ability Register: Address 7.19†

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner Next Page | 1 = Next Page ability | RO | | |
| E | Link Partner Extended Next Page Acknowledge | 1 = Link Partner acknowledges receipt of corresponding page | RO | | Acknowledge is used by the autonegotiation function to indicate that a device has successfully received its link partners link code word. |
| D | Link Partner Message Page | 1 = Message Page<br>0 = Unformatted page | RO | | |

*Table 6.9.15* **Autonegotiation Link Partner Extended Next Page Ability Register: Address 7.19**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| C | Link Partner Acknowledge 2 | 1 = Link Partner acknowledges that they *can* comply with the current Next Page<br>0 = Link Partner *cannot* comply with the current Next Page | RO | | |
| B | Link Partner Toggle | Value of link partner's toggle bit | RO | | Set to the opposite of the corresponding bit in the previous page. |
| A:0 | Link Partner Message Code Field [A:0] | [A:0] = Message Code Field:<br><br>0x0 = Reserved<br>0x1 = Null message<br>0x2 -> 0x3 Reserved Expansion message<br>0x4 = Remote Fault details message<br>0x5 = OUI message<br>0x6 = PHY ID message<br>0x7 = 100BASE-T2 message<br>0x8 = 1000BASE-T message<br>0x9 = 10GBASE-T message | RO | | Interpreted as message code (see 802.3 Appendix 28C) if Message Page bit is set to one (7.16:1). Otherwise interpreted as an unformatted code field. |

*Table 6.9.15* **Autonegotiation Link Partner Extended Next Page Ability Register: Address 7.19** (continued)

### 6.9.16 Autonegotiation Link Partner Extended Next Page Unformatted Code Register 1: Address 7.1A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Unformatted Code Field 1 [F:0] | [F:0] = Unformatted Code Field 1 [15:0] | RO | | |

*Table 6.9.16* **Autonegotiation Link Partner Extended Next Page Unformatted Code Register 1: Address 7.1A**

† This register, along with 7.1A and 7.1B, are used to store the received Next Pages. If an Extended Next Page is used, it is stored in 7.19 -> 7.1B.

### 6.9.17 Autonegotiation Link Partner Extended Next Page Unformatted Code Register 2: Address 7.1B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Unformatted Code Field 2 [F:0] | [F:0] = Unformatted Code Field 2 [15:0] | RO | | |

*Table 6.9.17* **Autonegotiation Link Partner Extended Next Page Unformatted Code Register 2: Address 7.1B**

### 6.9.18 Autonegotiation 10GBASE-T Control Register: Address 7.20

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | MASTER-SLAVE Manual Configuration Enable | 1 = Enables MASTER-SLAVE Manual configuration<br>0 = Disables MASTER-SLAVE Manual configuration | R/W PD | 0 | |
| E | MASTER-SLAVE Configuration | 1 = MASTER<br>0 = SLAVE | R/W PD | 0 | |
| D | Port Type | 1 = Multiport device<br>0 = Single port device | R/W PD | 0 | |
| C | 10GBASE-T Ability | 1 = Advertises PHY as 10GBASE-T capable<br>0 = Do *not* advertise PHY as 10GBASE-T capable | R/W PD | 1 | |
| B | 40GBASE-T Ability | 1 = Advertises PHY as 40GBASE-T capable<br>0 = Do *not* advertise PHY as 40GBASE-T capable | R/W PD | 0 | |
| A | 25GBASE-T Ability | 1 = Advertises PHY as 25GBASE-T capable<br>0 = Do *not* advertise PHY as 25GBASE-T capable | R/W PD | 0 | |

*Table 6.9.18* **Autonegotiation 10GBASE-T Control Register: Address 7.20**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9 | 25GBASE-T Fast Retrain Ability | 1 = Advertises PHY as 25GBASE-T fast retrain capable<br>0 = Do *not* advertise PHY as 25GBASE-T fast retrain capable | R/W PD | 0 | |
| 8 | 5GBASE-T Ability | 1 = Advertises PHY as 5GBASE-T capable<br>0 = Do *not* advertise PHY as 5GBASE-T capable | R/W PD | 1 | |
| 7 | 2.5GBASE-T Ability | 1 = Advertises PHY as 2.5GBASE-T capable<br>0 = Do *not* advertise PHY as 2.5GBASE-T capable | R/W PD | 1 | |
| 6 | 5GBASE-T Fast Retrain Ability | 1 = Advertises PHY as 5GBASE-T fast retrain capable<br>0 = Do *not* advertise PHY as 5GBASE-T fast retrain capable | R/W PD | 0 | |
| 5 | 2.5GBASE-T Fast Retrain Ability | 1 = Advertises PHY as 2.5GBASE-T fast retrain capable<br>0 = Do *not* advertise PHY as 2.5GBASE-T fast retrain capable | R/W PD | 0 | |
| 4 | Reserved_20_4 | Reserved bit 4 | R/W PD | 0 | |
| 3 | 40GBASE-T Fast Retrain Ability | 1 = Advertises PHY as 40GBASE-T fast retrain capable<br>0 = Do *not* advertise PHY as 40GBASE-T fast retrain capable | R/W PD | 0 | |

*Table 6.9.18* **Autonegotiation 10GBASE-T Control Register: Address 7.20** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | LD PMA Training Reset Request | 1 = Local device requests that Link Partner reset PMA training PRBS every frame<br>0 = Local device requests that Link Partner run PMA training PRBS continuously | R/W PD | 0 | |
| 1 | LD Fast Retrain Ability | 1 = Advertise PHY as 10GBASE-T fast retrain capable<br>0 = Do *not* advertise PHY as 10GBASE-T fast retrain capable | R/W PD | 0 | |
| 0 | LD Loop Timing Ability | 1 = Advertise PHY as capable of loop timing<br>0 = Do *not* advertise PHY as capable of loop timing | R/W PD | 1 | |

*Table 6.9.18* **Autonegotiation 10GBASE-T Control Register: Address 7.20** (continued)

### 6.9.19 Autonegotiation 10GBASE-T Status Register: Address 7.21

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | MASTER-SLAVE Configuration Fault | 1 = MASTER-SLAVE configuration fault | LH | | |
| E | MASTER-SLAVE Configuration Resolution | 1 = Local PHY resolved to MASTER<br>0 = Local PHY resolved to SLAVE | RO | | |
| D | Local Receiver Status | 1 = Local receiver OK<br>0 = Local receiver is *not* OK | RO | | Set by microcontroller |
| C | Remote Receiver Status | 1 = Remote receiver OK<br>0 = Remote receiver is *not* OK | RO | | Set by microcontroller |

*Table 6.9.19* **Autonegotiation 10GBASE-T Status Register: Address 7.21**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| B | Link Partner 10GBASE-T Ability | 1 = Link partner is 10GBASE-T capable<br>0 = Link partner is *not* 10GBASE-T capable | RO | | This bit is only valid when the Page received bit 7.1.6 is set to 1. |
| A | Link Partner Loop Timing Ability | 1 = Link partner is capable of loop timing<br>0 = Link partner is *not* capable of loop timing | RO | | |
| 9 | Link Partner Training Reset Request | 1 = Link partner has requested that PMA PRBS training be reset every frame<br>0 = Link partner has requested that PMA PRBS training run continuously. | RO | | |
| 8 | Link Partner 40GBASE-T Ability | 1 = Link partner is 40GBASE-T capable<br>0 = Link partner is *not* 40GBASE-T capable | RO | | |
| 7 | Link Partner 25GBASE-T Ability | 1 = Link partner is 25GBASE-T capable<br>0 = Link partner is *not* 25GBASE-T capable | RO | | |
| 6 | Link Partner 5GBASE-T Ability | 1 = Link partner is 5GBASE-T capable<br>0 = Link partner is *not* 5GBASE-T capable | RO | | |
| 5 | Link Partner 2.5GBASE-T Ability | 1 = Link partner is 2.5GBASE-T capable<br>0 = Link partner is *not* 2.5GBASE-T capable | RO | | |
| 4 | Link Partner 5GBASE-T Fast Retrain Ability | 1 = Link partner is 5GBASE-T fast retrain capable<br>0 = Link partner is *not* 5GBASE-T fast retrain capable | RO | | |
| 3 | Link Partner 2.5GBASE-T Fast Retrain Ability | 1 = Link partner is 2.5GBASE-T fast retrain capable<br>0 = Link partner is *not* 2.5GBASE-T fast retrain capable | RO | | |

*Table 6.9.19* **Autonegotiation 10GBASE-T Status Register: Address 7.21** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Link Partner 25GBASE-T Fast Retrain Ability | 1 = Link partner is 25GBASE-T fast retrain capable<br>0 = Link partner is *not* 25GBASE-T fast retrain capable | RO | | |
| 1 | Link Partner 10GBASE-T Fast Retrain Ability | 1 = Link partner is capable of 10GBASE-T fast retrain<br>0 = Link partner is *not* capable of 10GBASE-T fast retrain. | RO | | |
| 0 | Link Partner 40GBASE-T Fast Retrain Ability | 1 = Link partner is capable of 40GBASE-T fast retrain<br>0 = Link partner is *not* capable of 40GBASE-T fast retrain. | RO | | |

*Table 6.9.19* **Autonegotiation 10GBASE-T Status Register: Address 7.21** (continued)

### 6.9.20 Autonegotiation Reserved 22 Register: Address 7.22

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_22 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.20* **Autonegotiation Reserved 22 Register: Address 7.22**

### 6.9.21 Autonegotiation Reserved 23 Register: Address 7.23

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_23 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.21* **Autonegotiation Reserved 23 Register: Address 7.23**

### 6.9.22 Autonegotiation Reserved 31 Register: Address 7.31

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_31 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.22* **Autonegotiation Reserved 31 Register: Address 7.31**

### 6.9.23 Autonegotiation Reserved 32 Register: Address 7.32

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_32 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.23* **Autonegotiation Reserved 32 Register: Address 7.32**

### 6.9.24 Autonegotiation EEE Advertisement Register: Address 7.3C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved_3C [F:7] | Reserved bits 15 to 7 | R/W | 0x000 | |
| 6 | 10GBASE-KR EEE | 1 = Advertises that the 10GBASE-KR has EEE capability<br>0 = Does *not* advertise that the 10GBASE-KR has EEE capability | R/W | 0 | |
| 5 | 10GBASE-KX4 EEE | 1 = Advertises that the 10GBASE-KX4 has EEE capability<br>0 = Does *not* advertise that the 10GBASE-KX4 has EEE capability | R/W | 0 | |
| 4 | 1000BASE-KX EEE | 1 = Advertises that the 1000BASE-KX has EEE capability<br>0 = Does *not* advertise that the 1000BASE-KX has EEE capability | R/W | 0 | |

*Table 6.9.24* **Autonegotiation EEE Advertisement Register: Address 7.3C**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | 10GBASE-T EEE | 1 = Advertises that the 10GBASE-T has EEE capability<br>0 = Does *not* advertise that the 10GBASE-T has EEE capability | R/W | 1 | |
| 2 | 1000BASE-T EEE | 1 = Advertises that the 1000BASE-T has EEE capability<br>0 = Does *not* advertise that the 1000BASE-T has EEE capability | R/W | 1 | |
| 1 | 100BASE-TX EEE | 1 = Advertises that the 100BASE-TX has EEE capability<br>0 = Does *not* advertise that the 100BASE-TX has EEE capability | R/W | 0 | |
| 0 | Reserved_3C 0 | Reserved bit 0 | R/W | 0 | |

*Table 6.9.24* **Autonegotiation EEE Advertisement Register: Address 7.3C** (continued)

### 6.9.25 Autonegotiation EEE Link Partner Ability Register: Address 7.3D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved_3D [F:7] | Reserved bits 15 to 7 | RO | | |
| 6 | Link Partner 10GBASE-KR EEE | 1 = Link partner advertises that its 10GBASE-KR has EEE capability<br>0 = Link partner advertises that its 10GBASE-KR does *not* have EEE capability | RO | | |
| 5 | Link Partner 10GBASE-KX4 EEE | 1 = Link partner advertises that its 10GBASE-KX4 has EEE capability<br>0 = Link partner advertises that its 10GBASE-KX4 does *not* have EEE capability | RO | | |

*Table 6.9.25* **Autonegotiation EEE Link Partner Ability Register: Address 7.3D**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | Link Partner 1000BASE-KX EEE | 1 = Link partner advertises that its 1000BASE-KX has EEE capability<br>0 = Link partner advertises that its 1000BASE-KX does *not* have EEE capability | RO | | |
| 3 | Link Partner 10GBASE-T EEE | 1 = Link partner advertises that its 10GBASE-T has EEE capability<br>0 = Link partner advertises that its 10GBASE-T does *not* have EEE capability | RO | | |
| 2 | Link Partner 1000BASE-T EEE | 1 = Link partner advertises that its 1000BASE-T has EEE capability<br>0 = Link partner advertises that its 1000BASE-T does *not* have EEE capability | RO | | |
| 1 | Link Partner 100BASE-TX EEE | 1 = Link partner advertises that its 100BASE-TX has EEE capability<br>0 = Link partner advertises that its 100BASE-TX does *not* have EEE capability | RO | | |
| 0 | Reserved_3D 0 | Reserved bit 0 | RO | | |

*Table 6.9.25* **Autonegotiation EEE Link Partner Ability Register: Address 7.3D** (continued)

### 6.9.26 Autonegotiation EEE Advertisement 2 Register: Address 7.3E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved_3E [F:2] | Reserved bits 15 to 2 | R/W | 0x0000 | |
| 1 | 5GBASE-T EEE | 1 = Advertises that the 5BASE-T has EEE capability<br>0 = Advertises that the 5BASE-T does *not* have EEE capability | R/W | 1 | |
| 0 | 2.5GBASE-T EEE | 1 = Advertises that the 2.5GBASE-T has EEE capability<br>0 = Advertises that the 2.5GBASE-T does *not* have EEE capability | R/W | 1 | |

*Table 6.9.26* **Autonegotiation EEE Advertisement 2 Register: Address 7.3E**

### 6.9.27 Autonegotiation EEE Link Partner Ability 2 Register: Address 7.3F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved_3F [F:2] | Reserved bits 15 to 2 | RO | | |
| 1 | Link Partner 5GBASE-T EEE | 1 = Link partner advertises that its 5BASE-T has EEE capability<br>0 = Link partner advertises that its 5BASE-T does *not* have EEE capability | RO | | |
| 0 | Link Partner 2.5GBASE-T EEE | 1 = Link partner advertises that its 2.5GBASE-T has EEE capability<br>0 = Link partner advertises that its 2.5GBASE-T does *not* have EEE capability | RO | | |

*Table 6.9.27* **Autonegotiation EEE Link Partner Ability 2 Register: Address 7.3F**

### 6.9.28 Autonegotiation 10GBASE-T Control 2 Register: Address 7.40

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved_40 [F:4] | Reserved bits 15 to 4 | R/W | 0x000 | |
| 3 | 2.5GBASE-T THP Bypass Request | 1 = Requests to reset THP during fast retrain for 2.5GBASE-T<br>0 = Requests *not* to reset THP during fast retrain for 2.5GBASE-T | R/W PD | 0 | |
| 2 | 5GBASE-T THP Bypass Request | 1 = Requests to reset THP during fast retrain for 5GBASE-T<br>0 = Requests *not* to reset THP during fast retrain for 5GBASE-T | R/W PD | 0 | |
| 1 | 25GBASE-T THP Bypass Request | 1 = Requests to reset THP during fast retrain for 25GBASE-T<br>0 = Requests *not* to reset THP during fast retrain for 25GBASE-T | R/W PD | 0 | |
| 0 | 40GBASE-T THP Bypass Request | 1 = Requests to reset THP during fast retrain for 40GBASE-T<br>0 = Requests *not* to reset THP during fast retrain for 40GBASE-T | R/W PD | 0 | |

*Table 6.9.28* **Autonegotiation 10GBASE-T Control 2 Register: Address 7.40**

### 6.9.29 Autonegotiation 10GBASE-T Status 2 Register: Address 7.41

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved_41 [F:4] | Reserved bits 15 to 4 | RO | | |
| 3 | Link Partner 2.5GBASE-T THP Bypass Request | 1 = Link Partner requests to reset THP during fast retrain for 2.5GBASE-T<br>0 = No Link Partner requests to reset THP during fast retrain for 2.5GBASE-T | RO | | |
| 2 | Link Partner 5GBASE-T THP Bypass Request | 1 = Link Partner requests to reset THP during fast retrain or 5GBASE-T<br>0 = No Link Partner requests to reset THP during fast retrain for 5GBASE-T | RO | | |
| 1 | Link Partner 25GBASE-T THP Bypass Request | 1 = Link Partner requests to reset THP during fast retrain for 25GBASE-T<br>0 = No Link Partner requests to reset THP during fast retrain for 25GBASE-T | RO | | |
| 0 | Link Partner 40GBASE-T THP Bypass Request | 1 = Link Partner requests to reset THP during fast retrain for 40GBASE-T<br>0 = No Link Partner requests to reset THP during fast retrain for 40GBASE-T | RO | | |

*Table 6.9.29* **Autonegotiation 10GBASE-T Status 2 Register: Address 7.41**

### 6.9.30 Autonegotiation Reserved 42 Register: Address 7.42

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_42 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.30* **Autonegotiation Reserved 42 Register: Address 7.42**

### 6.9.31 Autonegotiation Reserved 43 Register: Address 7.43

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_43 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.31* **Autonegotiation Reserved 43 Register: Address 7.43**

### 6.9.32 Autonegotiation Reserved 44 Register: Address 7.44

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_44 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.32* **Autonegotiation Reserved 44 Register: Address 7.44**

### 6.9.33 Autonegotiation Reserved 45 Register: Address 7.45

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved_45 [F:0] | Reserved bits 15 to 0 | R/W | 0x0000 | |

*Table 6.9.33* **Autonegotiation Reserved 45 Register: Address 7.45**

### 6.9.34 KR0 Autonegotiation Control: Address 7.C200

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reset | 1 = Autonegotiation reset<br>0 = Normal operation | R/W<br>SC | 1 | |
| E:D | Reserved 0 [1:0] | Reserved for future use | R/W<br>PD | 0x0 | |
| C | Autonegotiation Enable | 1 = Enables autonegotiation<br>0 = Disables autonegotiation | R/W<br>PD | 0 | |
| B:A | Reserved 1 [1:0] | Reserved for future use | R/W<br>PD | 0x0 | |
| 9 | Autonegotiation Restart | 1 = Restarts autonegotiation<br>0 = Normal operation | R/W<br>SC | 0 | |
| 8:0 | Reserved 2 [8:0] | Reserved for future use | R/W<br>PD | 0x000 | |

*Table 6.9.34* **KR0 Autonegotiation Control: Address 7.C200**

### 6.9.35 KR0 Autonegotiation Status: Address 7.C201

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved 0 [5:0] | Reserved for future use | R/W PD | 0x00 | |
| 9 | Parallel Detection Fault | 1 = Fault detected<br>0 = No fault detected | LH | | |
| 8:7 | Reserved 1 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| 6 | Page Received | 1 = A new DME page has been received<br>0 = Normal operation | LH | | |
| 5 | Autonegotiation Complete | 1 = Autonegotiation complete<br>0 = Normal operation | LH | | |
| 4 | Reserved 2 | Reserved for future use | R/W PD | 0 | |
| 3 | Autonegotiation Ability | 1 = PHY is able to perform autonegotiation<br>0 = PHY is *not* able to perform autonegotiation | ROS | 1 | Always set as 1, as the local device has autonegotiation ability. |
| 2:1 | Reserved 3 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| 0 | Link Partner Autonegotiation Ability | 1 = Link partner is able to perform autonegotiation<br>0 = Link partner is *not* able to perform autonegotiation | ROS | 0 | |

*Table 6.9.35* **KR0 Autonegotiation Status: Address 7.C201**

### 6.9.36 KR0 Autonegotiation Advertisement Word 1: Address 7.C210

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Next Page | 1 = Next Page ability<br>0 = Next Page ability not supported or not engaged | R/W PD | 0 | |
| E | Acknowledge | 1 = Acknowledge<br>0 = No fault detected | R/W PD | 0 | The Acknowledge (Ack) is used by the Autonegotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. |
| D | Remote Fault | 1 = Remote Fault | R/W | 0 | The Remote Fault (RF) bit provides a standard transport mechanism for transmitting simple fault information. When the RF bit in the received base link code word is set to 1, the RF bit is set to 1. |
| C | Reserved 0 | Reserved for future use | R/W PD | 0 | |
| B:A | Pause Capability [1:0] | Bit B: PAUSE operation for full duplex links<br>Bit A: Asymmetric PAUSE operation for full duplex links | R/W PD | 0x0 | |

*Table 6.9.36* **KR0 Autonegotiation Advertisement Word 1: Address 7.C210**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9:5 | Echoed Nonce [4:0] | Echoed nonce | R/W PD | 0x00 | |
| 4:0 | Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | R/W PD | 0x01 | Field should always be set to 0x01 as the PHY is only capable of handling 802.3 Ethernet. |

*Table 6.9.36* **KR0 Autonegotiation Advertisement Word 1: Address 7.C210** (continued)

### 6.9.37 KR0 Autonegotiation Advertisement Word 2: Address 7.C211

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Technology Ability Bits A3 to A10 [7:0] | Reserved for future technology | R/W PD | 0x00 | |
| 7 | Technology Ability Bit A2 | 1 = 10GBASE-KR is supported<br>0 = 10GBASE-KR is *not* supported | R/W PD | 1 | |
| 6 | Technology Ability Bit A1 | 1 = 10GBASE-KX4 is supported<br>0 = 10GBASE-KX4 is *not* supported | R/W PD | 0 | |
| 5 | Technology Ability Bit A0 | 1 = 10GBASE-KX is supported<br>0 = 10GBASE-KX is not supported | R/W PD | 1 | |
| 4:0 | Transmitted Nonce [4:0] | Transmitted nonce | R/W PD | 0x00 | |

*Table 6.9.37* **KR0 Autonegotiation Advertisement Word 2: Address 7.C211**

### 6.9.38 KR0 Autonegotiation Advertisement Word 3: Address 7.C212

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | FEC Requested | 1 = Enables 10GBASE-KR FEC ability.<br>0 = Disables 10GBASE-KR FEC ability. | R/W PD | 0 | |
| E | FEC Ability | 1 = 10GBASE-KR PHY has FEC capability.<br>0 = 10GBASE-KR PHY does *not* have FEC capability. | R/W PD | 0 | |
| D:0 | Technology Ability Bits A11 to A24 [D:0] | Reserved for future technology | R/W PD | 0x0000 | |

*Table 6.9.38* **KR0 Autonegotiation Advertisement Word 3: Address 7.C212**

### 6.9.39 KR0 Link Partner Autonegotiation Advertisement Word 1: Address 7.C213

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner Next Page | 1 = Next Page ability<br>0 = Next Page ability *not* supported or *not* engaged | RO | | |
| E | Link Partner Acknowledge | 1 = Acknowledge<br>0 = No fault detected | RO | | The Acknowledge (Ack) is used by the Autonegotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. |

*Table 6.9.39* **KR0 Link Partner Autonegotiation Advertisement Word 1: Address 7.C213**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Link Partner Remote Fault | 1 = Remote Fault | RO | | The Remote Fault (RF) bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1, the RF bit is set to 1. |
| C | Reserved 0 | Reserved for future use | RO | | |
| B:A | Link Partner Pause Capability [1:0] | Bit B: PAUSE operation for full duplex links<br>Bit A: Asymmetric PAUSE operation for full duplex links | RO | | |
| 9:5 | Link Partner Echoed Nonce [4:0] | Echoed nonce | RO | | |
| 4:0 | Link Partner Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | RO | | Field should always be set to 0x01 as the PHY is only capable of handling 802.3 Ethernet. |

*Table 6.9.39* **KR0 Link Partner Autonegotiation Advertisement Word 1: Address 7.C213** (continued)

### 6.9.40 KR0 Link Partner Autonegotiation Advertisement Word 2: Address 7.C214

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Link Partner Technology Ability bits A3 to A10 [7:0] | Reserved for future technology | RO | | |
| 7 | Link Partner Technology Ability bit A2 | 1 = 10GBASE-KR is supported<br>0 = 10GBASE-KR is *not* supported | RO | | |
| 6 | Link Partner Technology Ability bit A1 | 1 = 10GBASE-KX4 is supported<br>0 = 10GBASE-KX4 is *not* supported | RO | | |
| 5 | Link Partner Technology Ability Bit A0 | 1 = 10GBASE-KX is supported<br>0 = 10GBASE-KX is *not* supported | RO | | |
| 4:0 | Link Partner Transmitted Nonce [4:0] | Transmitted nonce | RO | | |

*Table 6.9.40* **KR0 Link Partner Autonegotiation Advertisement Word 2: Address 7.C214**

### 6.9.41 KR0 Link Partner Autonegotiation Advertisement Word 3: Address 7.C215

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner FEC Requested | 1 = Enables 10GBASE-KR FEC ability.<br>0 = Disables 10GBASE-KR FEC ability. | RO | | |
| E | Link Partner FEC Ability | 1 = 10GBASE-KR PHY has FEC capability.<br>0 = 10GBASE-KR PHY does *not* have FEC capability. | RO | | |
| D:0 | Link Partner Technology Ability Bits A11 to A24 [D:0] | Reserved for future technology | RO | | |

*Table 6.9.41* **KR0 Link Partner Autonegotiation Advertisement Word 3: Address 7.C215**

### 6.9.42 KR0 Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C216

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 0 [F:0] | Extended Next Page bits [F:0] | R/W PD | 0x0000 | |

*Table 6.9.42* **KR0 Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C216**

### 6.9.43 KR0 Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C217

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 1 [1F:10] | Extended Next Page bits [1F:10] | R/W PD | 0x0000 | |

*Table 6.9.43* **KR0 Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C217**

### 6.9.44 KR0 Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C218

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 2 [2F:20] | Extended Next Page bits [2F:20] | R/W PD | 0x0000 | |

*Table 6.9.44* **KR0 Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C218**

### 6.9.45 KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C219

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 0 [F:0] | Extended Next Page bits [F:0] | RO | | |

*Table 6.9.45* **KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C219**

### 6.9.46 KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C21A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 1 [1F:10] | Extended Next Page bits [1F:10] | RO | | |

*Table 6.9.46* **KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C21A**

### 6.9.47 KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C21B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 2 [2F:20] | Extended Next Page bits [2F:20] | RO | | |

*Table 6.9.47* **KR0 Link Partner Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C21B**

### 6.9.48 KR1 Autonegotiation Control: Address 7.C300

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reset | 1 = Autonegotiation reset<br>0 = Normal operation | R/WSC | 1 | |
| E:D | Reserved 0 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| C | Autonegotiation Enable | 1 = Enable autonegotiation<br>0 = Disable autonegotiation | R/W PD | 0 | |
| B:A | Reserved 1 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| 9 | Autonegotiation Restart | 1 = Restart autonegotiation<br>0 = Normal operation | R/WSC | 0 | |
| 8:0 | Reserved 2 [8:0] | Reserved for future use | R/W PD | 0x000 | |

*Table 6.9.48* **KR1 Autonegotiation Control: Address 7.C300**

### 6.9.49 KR1 Autonegotiation Status: Address 7.C301

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved 0 [5:0] | Reserved for future use | R/W PD | 0x00 | |
| 9 | Parallel Detection Fault | 1 = Fault detected<br>0 = No fault detected | LH | | |
| 8:7 | Reserved 1 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| 6 | Page Received | 1 = A new DME page has been received<br>0 = Normal operation | LH | | |
| 5 | Autonegotiation Complete | 1 = Autonegotiation complete<br>0 = Normal operation | LH | | |
| 4 | Reserved 2 | Reserved for future use | R/W PD | 0 | |
| 3 | Autonegotiation Ability | 1 = PHY is able to perform autonegotiation<br>0 = PHY is *not* able to perform autonegotiation | ROS | 1 | Always set as 1, as the local device has autonegotiation ability. |
| 2:1 | Reserved 3 [1:0] | Reserved for future use | R/W PD | 0x0 | |
| 0 | Link Partner Autonegotiation Ability | 1 = Link partner is able to perform autonegotiation<br>0 = Link partner is *not* able to perform autonegotiation | ROS | 0 | |

*Table 6.9.49* **KR1 Autonegotiation Status: Address 7.C301**

### 6.9.50 KR1 Autonegotiation Advertisement Word 1: Address 7.C310

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Next Page | 1 = Next Page ability supported<br>0 = Next Page ability *not* supported or *not* engaged | R/W PD | 0 | |
| E | Acknowledge | 1 = Acknowledge<br>0 = No fault detected | R/W PD | 0 | The Acknowledge (Ack) is used by the Autonegotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. |
| D | Remote Fault | 1 = Remote Fault | R/W | 0 | The Remote Fault (RF) bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base is set to 1. |
| C | Reserved 0 | Reserved for future use | R/W PD | 0 | |
| B:A | Pause Capability [1:0] | Bit B: PAUSE operation for full duplex links<br>Bit A: Asymmetric PAUSE operation for full duplex links | R/W PD | 0x0 | |

*Table 6.9.50* **KR1 Autonegotiation Advertisement Word 1: Address 7.C310**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9:5 | Echoed Nonce [4:0] | Echoed nonce | R/W PD | 0x00 | |
| 4:0 | Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | R/W PD | 0x01 | Field should always be set to 0x01 as the PHY is only capable of handling 802.3 Ethernet. |

*Table 6.9.50* **KR1 Autonegotiation Advertisement Word 1: Address 7.C310** (continued)

### 6.9.51 KR1 Autonegotiation Advertisement Word 2: Address 7.C311

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Technology Ability Bits A3 to A10 [7:0] | Reserved for future technology | R/W PD | 0x00 | |
| 7 | Technology Ability Bit A2 | 1 = 10GBASE-KR is supported<br>0 = 10GBASE-KR is *not* supported | R/W PD | 1 | |
| 6 | Technology Ability Bit A1 | 1 = 10GBASE-KX4 is supported<br>0 = 10GBASE-KX4 is *not* supported | R/W PD | 0 | |
| 5 | Technology Ability Bit A0 | 1 = 10GBASE-KX is supported<br>0 = 10GBASE-KX is *not* supported | R/W PD | 1 | |
| 4:0 | Transmitted Nonce [4:0] | Transmitted nonce | R/W PD | 0x00 | |

*Table 6.9.51* **KR1 Autonegotiation Advertisement Word 2: Address 7.C311**

### 6.9.52 KR1 Autonegotiation Advertisement Word 3: Address 7.C312

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | FEC Requested | 1 = Enables 10GBASE-KR FEC ability.<br>0 = Disables 10GBASE-KR FEC ability. | R/W PD | 0 | |
| E | FEC Ability | 1 = 10GBASE-KR PHY has FEC capability.<br>0 = 10GBASE-KR PHY does *not* have FEC capability. | R/W PD | 0 | |
| D:0 | Technology Ability Bits A11 to A24 [D:0] | Reserved for future technology | R/W PD | 0x0000 | |

*Table 6.9.52* **KR1 Autonegotiation Advertisement Word 3: Address 7.C312**

### 6.9.53 KR1 Link Partner Autonegotiation Advertisement Word 1: Address 7.C313

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner Next Page | 1 = Next Page ability<br>0 = Next Page ability *not* supported or *not* engaged | RO | | |
| E | Link Partner Acknowledge | 1 = Acknowledge<br>0 = No fault detected | RO | | The Acknowledge (Ack) is used by the Autonegotiation function to indicate that a device has successfully received its Link Partner's Link Code Word. |

*Table 6.9.53* **KR1 Link Partner Autonegotiation Advertisement Word 1: Address 7.C313**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Link Partner Remote Fault | 1 = Remote Fault | RO | | The Remote Fault (RF) bit provides a standard transport mechanism for the transmission of simple fault information. When the RF bit in the received base link code word is set to 1, the RF bit is set to 1. |
| C | Reserved 0 | Reserved for future use | RO | | |
| B:A | Link Partner Pause Capability [1:0] | Bit B: PAUSE operation for full duplex links<br>Bit A: Asymmetric PAUSE operation for full duplex links | RO | | |
| 9:5 | Link Partner Echoed Nonce [4:0] | Echoed nonce | RO | | |
| 4:0 | Link Partner Selector Field [4:0] | This defines the device compatibility:<br>0x00 = Reserved<br>0x01 = IEEE 802.3<br>0x02 = IEEE 802.9 ISLAN-16T<br>0x03 = IEEE 802.5<br>0x04 = IEEE 1394<br>0x05 -> 0x1F = Reserved | RO | | Field should always be set to 0x01 as the PHY is only capable of handling 802.3 Ethernet. |

*Table 6.9.53* **KR1 Link Partner Autonegotiation Advertisement Word 1: Address 7.C313** (continued)

### 6.9.54 KR1 Link Partner Autonegotiation Advertisement Word 2: Address 7.C314

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Link Partner Technology Ability Bits A3 to A10 [7:0] | Reserved for future technology | RO | | |
| 7 | Link Partner Technology Ability Bit A2 | 1 = 10GBASE-KR is supported<br>0 = 10GBASE-KR is *not* supported | RO | | |
| 6 | Link Partner Technology Ability Bit A1 | 1 = 10GBASE-KX4 is supported<br>0 = 10GBASE-KX4 is *not* supported | RO | | |
| 5 | Link Partner Technology Ability Bit A0 | 1 = 10GBASE-KX is supported<br>0 = 10GBASE-KX is *not* supported | RO | | |
| 4:0 | Link Partner Transmitted Nonce [4:0] | Transmitted nonce | RO | | |

*Table 6.9.54* **KR1 Link Partner Autonegotiation Advertisement Word 2: Address 7.C314**

### 6.9.55 KR1 Link Partner Autonegotiation Advertisement Word 3: Address 7.C315

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner FEC Requested | 1 = Enables 10GBASE-KR FEC ability<br>0 = Disables 10GBASE-KR FEC ability | RO | | |
| E | Link Partner FEC Ability | 1 = 10GBASE-KR PHY has FEC capability<br>0 = 10GBASE-KR PHY does *not* have FEC capability | RO | | |
| D:0 | Link Partner Technology Ability Bits A11 to A24 [D:0] | Reserved for future technology | RO | | |

*Table 6.9.55* **KR1 Link Partner Autonegotiation Advertisement Word 3: Address 7.C315**

### 6.9.56 KR1 Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C316

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 0 [F:0] | Extended Next Page bits [F:0] | R/W PD | 0x0000 | |

*Table 6.9.56* **KR1 Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C316**

### 6.9.57 KR1 Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C317

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 1 [1F:10] | Extended Next Page bits [1F:10] | R/W PD | 0x0000 | |

*Table 6.9.57* **KR1 Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C317**

### 6.9.58 KR1 Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C318

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Extended Next Page 2 [2F:20] | Extended Next Page bits [2F:20] | R/W PD | 0x0000 | |

*Table 6.9.58* **KR1 Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C318**

### 6.9.59 KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C319

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 0 [F:0] | Extended Next Page bits [F:0] | RO | | |

*Table 6.9.59* **KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 1: Address 7.C319**

### 6.9.60 KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C31A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 1 [1F:10] | Extended Next Page bits [1F:10] | RO | | |

*Table 6.9.60* **KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 2: Address 7.C31A**

### 6.9.61 KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C31B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Link Partner Extended Next Page 2 [2F:20] | Extended Next Page bits [2F:20] | RO | | |

*Table 6.9.61* **KR1 Link Partner Autonegotiation Extended Next Page Advertisement Word 3: Address 7.C31B**

### 6.9.62 Autonegotiation Vendor Provisioning 1: Address 7.C400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | 1000BASE-T Full Duplex Ability | 1 = Advertises PHY as 1000BASE-T Full Duplex capable<br>0 = Does *not* advertise PHY as 1000BASE-T Full Duplex capable | R/W PD | 0 | |
| E | 1000BASE-T Half Duplex Ability | 1 = Advertises PHY as 1000BASE-T Half Duplex capable<br>0 = Does *not* advertise PHY as 1000BASE-T Half Duplex capable | R/W PD | 0 | |
| D | Short-Reach | 1 = Advertises PHY as operating in short-reach mode<br>0 = Does *not* advertise PHY as operating in short-reach mode | R/W PD | 0 | |
| C | AQRate Downshift Capability | 1 = Advertises PHY as supporting AQRate<br>0 = Does *not* advertise PHY as supporting AQRate | R/W PD | 0 | |

*Table 6.9.62* **Autonegotiation Vendor Provisioning 1: Address 7.C400**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| B | 5G | 1 = Advertises PHY as supporting 5G<br>0 = Does *not* advertise PHY as supporting 5G | R/W PD | 0 | |
| A | 2.5G | 1 = Advertises PHY as supporting 2.5G<br>0 = Does *not* advertise PHY as supporting 2.55G | R/W PD | 0 | |
| 9:7 | Reserved1 [2:0] | Reserved for future use | R/W PD | 0x0 | |
| 6 | Exchange PHY ID Information | 1 = Exchanges PHY ID Information | R/W PD | 1 | |
| 5 | User Provided Autonegotiation Data | 1 = User provides the Next Page or Extended Next Page data directly (7.16 -> 7.18), and the configuration info in 7.20 and 7.C400 is ignored<br>0 = Constructs the correct autonegotiation words based on the register settings of 7.10, 7.20, and 7.C400 | R/W PD | 0 | If bit is set, PHY attempts to use the user-provided autonegotiation words. If there is a mismatch (such as a legacy 1GBASE-T device attempting connect), then PHY attempts to construct a new set of autonegotiation words from the data provided in these words.<br><br>Otherwise, the PHY constructs the correct autonegotiation words based on the provisioned values. |

*Table 6.9.62* **Autonegotiation Vendor Provisioning 1: Address 7.C400** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | Automatic Downshift Enable | 1 = Enables automatic downshift<br>0 = Manual downshift | R/W PD | 1 | |
| 3:0 | Retry Attempts Before Downshift [3:0] | Denotes the number of retry attempts before downshift | R/W PD | 0x4 | If Automatic Downshifting is enabled, this is the number of retry attempts the PHY will make to connect at the maximum mutually acceptable rate, before removing this rate from the list and trying at the next lower rate. |

*Table 6.9.62* **Autonegotiation Vendor Provisioning 1: Address 7.C400** (continued)

### 6.9.63 Autonegotiation Reserved Vendor Provisioning 1: Address 7.C410

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved Provisioning 0 [4:0] | Reserved for future use | R/W PD | 0x00 | |
| A:8 | Semi-Cross Link Attempt Period [2:0] | Number of failed link attempts before trying semi cross | R/W PD | 0x0 | Set to zero (0) to disable semi-cross. Set to 0x7 to *always* use semi-cross. |
| 7 | WoL Mode | 0 = 100BASE-TX<br>1 = 1000BASE-T | R/W PD | 0 | Bit indicates if the AQR107-AQR109 is going to go into 100BASE-TX or 1000BASE-T Wake-On-LAN operation. |
| 6 | WoL Enable | 1 = Enables Wake-On-LAN operation<br>0 = Normal Operation | R/W PD | 0 | Setting this bit enables Wake-On-LAN operation. In this state, power is minimized by turning all interfaces off except for the MDI receive path and the MDIO interface. |

*Table 6.9.63* **Autonegotiation Reserved Vendor Provisioning 1: Address 7.C410**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5:2 | Extra Page Count [3:0] | Number of extra pages to send at end of auto-negotiation sequence when link partner is a legacy gigabit PHY. | R/W PD | 0x0 | Intervals between pages for GbE PHYs may be much longer. When this is the case, the link partner may still be in auto-negotiation when the AQR107-AQR109 has started training. This can confuse the link partner MDI/MDI-X state machine, and the sending of extra pages aids to resolve this problem. |
| 1:0 | MDI/MDI-X Control [1:0] | 0x0 = Automatic MDI/MDI-X operation<br>0x1 = Manual MDI<br>0x2 = Manual MDI-X<br>0x3 = Reserved | R/W PD | 0x0 | These bits are used to force a manual MDI or MDI-X configuration. |

*Table 6.9.63* **Autonegotiation Reserved Vendor Provisioning 1: Address 7.C410** (continued)

### 6.9.64 Autonegotiation Vendor Status 1: Address 7.C800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3:1 | Connect Rate [2:0] | The rate the PHY connected or attempting to connect at:<br>0x5 = 5G<br>0x4 = 2.5G<br>0x3 = 10GBASE-T<br>0x2 = 1000BASE-T<br>0x1 = 100BASE-TX<br>0x0 = 10BASE-T | RO | | This field is used in conjunction with Connection State in "Autonegotiation Reserved Vendor Status 1: Address 7.C810" to indicated the rate that the PHY is either connected or attempting to connect at. |
| 0 | Connect Type | The duplex method that the PHY is either connected or attempting to connect at:<br>1 = Full Duplex<br>0 = Half-Duplex | RO | | This field is used in conjunction with Connection State in "Autonegotiation Reserved Vendor Status 1: Address 7.C810" to indicated the duplex method the PHY is either connected or attempting to connect at. |

*Table 6.9.64* **Autonegotiation Vendor Status 1: Address 7.C800**

### 6.9.65 Autonegotiation Reserved Vendor Status 1: Address 7.C810

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Energy On Line | 1 = Energy detected on line<br>0 = No energy detected on line | RO | | Bit indicates that the PHY has detected energy on the line. Specifically, when MDI/MDI-X resolution has completed, this bit is true. This bit is set false before entering autonegotiation. |
| E | Device Present | 1 = Far-end Ethernet device present<br>0 = No far-end Ethernet device detected | RO | | If true, a far-end Ethernet device exists, as valid link pulses have been detected in the most recent autonegotiation session, or a valid Ethernet connection has been established.<br><br>If false, no connection is established, and the most recent attempt at autonegotiation failed to detect any valid link pulses. Specifically, when MDI/MDI-X resolution has completed, this bit is true. This bit is set false before entering autonegotiation. |

*Table 6.9.65* **Autonegotiation Reserved Vendor Status 1: Address 7.C810**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D:9 | Connection State [4:0] | The current state of the connection:<br>0x00 = Inactive (for example, high-impedance)<br>0x01 = Cable diagnostics<br>0x02 = Autonegotiation<br>0x03 = Training (10G and 1G only)<br>0x04 = Connected<br>0x05 = Fail (Autonegotiation Break Link)<br>0x06 = Test Mode<br>0x07 = Loopback Mode<br>0x08 = Low Power Mode<br>0x09 = Connected Wake-On-LAN Mode<br>0x0A = System Calibrating<br>0x0B = Cable Disconnected<br>0x0C -> 0x1E = Reserved<br>0x1F = Invalid | RO | | This field is used in conjunction with Connect Rate and Connect Type in "Autonegotiation Vendor Status 1: Address 7.C800" to indicate the current state that the PHY is in. |
| 8 | MDI/MDI-X | 0 = MDI<br>1 = MDI-X | RO | | When autonegotiation is completed, this register indicates whether the connection was made as an MDI or MDI-X connection. |
| 7 | Duplicate Link Partner Autonegotiation Ability | Link Partner is capable of Autonegotiation. | RO | | This is a duplicate of the bit at 07.0001.0. |
| 6:2 | Reserved Status 1 [6:2] | Reserved for future use | RO | | |
| 1 | Receive PAUSE Resolution | 1 = Receives PAUSE Enabled<br>0 = Receives PAUSE Disabled | RO | | PAUSE resolution from 28B-3. |
| 0 | Transmit PAUSE Resolution | 1 = Transmits PAUSE Enabled<br>0 = Transmits PAUSE Disabled | RO | | |

*Table 6.9.65* **Autonegotiation Reserved Vendor Status 1: Address 7.C810** (continued)

### 6.9.66 Autonegotiation Reserved Vendor Status 2: Address 7.C811

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Autonegotiation Attempts [F:0] | The number of autonegotiation attempts since the last successful connection (or power-up) | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero). It is cleared upon reset, or the completion of a successful connection. |

*Table 6.9.66* **Autonegotiation Reserved Vendor Status 2: Address 7.C811**

### 6.9.67 Autonegotiation Reserved Vendor Status 3: Address 7.C812

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Pulse Detected Status | 1 = Link Pulse Detected<br>0 = Link Pulse *not* Detected | RO | | |
| E:1 | Reserved State 3 [D:0] | Reserved for future use | RO | | |
| 0 | WoL Ready | 1 = Preparations for Wake-on-LAN mode are complete<br>0 = Wake-on-LAN mode has *not* been requested, or preparations for Wake-on-LAN mode are *not* yet complete | RO | | When the system enables Wake-on-LAN and restarts autonegotiation, the PHY firmware powers down blocks that are *not* needed for Wake-on-LAN mode, in preparation for switching to auxiliary supplies.<br><br>This status flag indicates that this work has been completed, and the system should confirm that this flag has been set before the switchover occurs. Note that this field is independent of the link state. |

*Table 6.9.67* **Autonegotiation Reserved Vendor Status 3: Address 7.C812**

### 6.9.68 Autonegotiation Reserved Vendor Status 4: Address 7.C813

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Autonegotiation Restarts Handled [F:0] | The number of line-side autonegotiation restart commands received. | RO | | This is a rolling counter (for example, upon saturation, it reverts to zero). It is cleared upon reset. |

*Table 6.9.68* **Autonegotiation Reserved Vendor Status 4: Address 7.C813**

### 6.9.69 Autonegotiation Reserved Vendor Status 5: Address 7.C814

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Autonegotiation Attempts Since Reset [F:0] | The number of autonegotiation attempts since the last PHY reset (or power-up) | RO | | Increments when the line-side goes back to ‘break-link’ state and then re-negotiates. This is a rolling counter (for example, upon saturation, it reverts to zero), that is cleared upon reset. |

*Table 6.9.69* **Autonegotiation Reserved Vendor Status 5: Address 7.C814**

### 6.9.70 Autonegotiation Transmit Vendor Alarms 1: Address 7.CC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | Autonegotiation Completed For Non-supported Rate | 1 = Autonegotiation has completed for a rate that is *not* supported by the AQR107-AQR109 | LH | | This means that the AQR107-AQR109 has completed autonegotiation, and was unable to agree on a rate that both could operate at. Indication should be ignored in case of Master/Slave resolution fault. |
| 2 | Autonegotiation Completed for Supported Rate | 1 = Autonegotiation has completed successfully for a rate that is supported by the AQR107-AQR109 | LH | | |
| 1 | Automatic Downshift | 1 = Automatic downshift has occurred | LH | | |
| 0 | Connection State Change | 1 = The connection state has changed | LH | | Interrupt indicates that a change in Connection State [D:B] in "Autonegotiation Reserved Vendor Status 1: Address 7.C810" on page 400. Note that this indicates any state change, versus 7.CC01.0 that indicates a connect or disconnect event has occurred. |

*Table 6.9.70* **Autonegotiation Transmit Vendor Alarms 1: Address 7.CC00**

### 6.9.71 Autonegotiation Transmit Vendor Alarms 2: Address 7.CC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Pulse Detect | 1 = Link Pulse Detected | LH | | |
| E:1 | Reserved Vendor Alarms 2 [D:0] | Reserved for future use | LH | | |
| 0 | Link Connect / Disconnect | 1 = MDI Link has either connected or disconnected | LH | | Indicates if the link has achieved a connect state, or was in a connect state and then disconnected. |

*Table 6.9.71* **Autonegotiation Transmit Vendor Alarms 2: Address 7.CC01**

### 6.9.72 Autonegotiation Standard Interrupt Mask 1: Address 7.D000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9 | Parallel Detection Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 8:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Extended Next Page Received Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 5 | Reserved | Internal reserved - do not modify | | | |
| 4 | Remote Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3 | Reserved | Internal reserved - do not modify | | | |
| 2 | Link Status Mask | 1 = Enable interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.72* **Autonegotiation Standard Interrupt Mask 1: Address 7.D000**

### 6.9.73 Autonegotiation Standard Interrupt Mask 2: Address 7.D001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | MASTER-SLAVE Configuration Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| E:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.73* **Autonegotiation Standard Interrupt Mask 2: Address 7.D001**

### 6.9.74 Autonegotiation Transmit Vendor Interrupt Mask 1: Address 7.D400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | Autonegotiation Completed For Non-supported Rate Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2 | Autonegotiation Completed for Supported Rate Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 1 | Automatic Downshift Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 0 | Connection State Change Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.9.74* **Autonegotiation Transmit Vendor Interrupt Mask 1: Address 7.D400**

### 6.9.75 Autonegotiation Transmit Vendor Interrupt Mask 2: Address 7.D401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Pulse Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| E:1 | Reserved Vendor Alarms 2 Mask [D:0] | Reserved for future use | R/W PD | 0x0000 | |
| 0 | Link Connect / Disconnect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.9.75* **Autonegotiation Transmit Vendor Interrupt Mask 2: Address 7.D401**

### 6.9.76 Autonegotiation Transmit Vendor Interrupt Mask 3: Address 7.D402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.76* **Autonegotiation Transmit Vendor Interrupt Mask 3: Address 7.D402**

### 6.9.77 Autonegotiation Receive Reserved Vendor Provisioning 1: Address 7.E410

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved Receive Provisioning 1 [E:0] | Reserved for future use | R/W PD | 0x0000 | |
| 0 | Disable 100BASE-TX Parallel Detection | 1 = Disables 100BASE-TX Parallel Detection<br>0 = Normal operation (100BASE-TX Parallel Detection enabled) | R/W PD | 0 | **Note:** If this bit is toggled during operation, autonegotiation *must* be restarted to ensure that this change takes effect. |

*Table 6.9.77* **Autonegotiation Receive Reserved Vendor Provisioning 1: Address 7.E410**

### 6.9.78 Autonegotiation Receive Reserved Vendor Provisioning 2: Address 7.E411

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved Receive Provisioning 2 [3:0] | Reserved for future use | R/W PD | 0x00 | |
| B | Downshift From 10G | Maximum advertised rate downshifted from 10G | R/W PD | 0 | |
| A | Downshift From 5G | Maximum advertised rate downshifted from 5G | R/W PD | 0 | |
| 9 | Downshift From 2.5G | Maximum advertised rate downshifted from 2.5G | R/W PD | 0 | |
| 8 | Downshift From 1G | Maximum advertised rate downshifted from 1G | R/W PD | 0 | |
| 7:4 | Max Advertised Rate [3:0] | Maximum advertised rate sent to the link partner through Autonegotiation:<br>0x5 = 5G<br>0x4 = 2.5G<br>0x3 = 10GBASE-T<br>0x2 = 1000BASE-T<br>0x1 = 100BASE-TX<br>0x0 = 10BASE-T | R/W PD | 0x0 | When downshift is enabled (7.C400.4), the maximum advertised rate may be different from the provisioned max rate listed in the autonegotiation capability registers (7.0020, 7.0010, 7.C400). |
| 3:0 | Max Rate Training Cnt [3:0] | Training attempt count at maximum advertised rate reported in 7.E411.7:4; this counter is set to zero for the first training attempt | R/W PD | 0x0 | |

*Table 6.9.78* **Autonegotiation Receive Reserved Vendor Provisioning 2: Address 7.E411**

### 6.9.79 Autonegotiation Receive Link Partner Status 1: Address 7.E820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Link Partner 1000BASE-T Full Duplex Ability | 1 = Link Partner is 1000BASE-T Full Duplex capable<br>0 = Link Partner is *not* 1000BASE-T Full Duplex capable | RO | | |
| E | Link Partner 1000BASE-T Half Duplex Ability | 1 = Link Partner is 1000BASE-T Half-Duplex capable<br>0 = Link Partner is *not* 1000BASE-T Half-Duplex capable | RO | | |
| D | Link Partner Short-Reach | 1 = Link Partner is operating in short-reach mode<br>0 = Link Partner is *not* operating in short-reach mode | RO | | |
| C | Link Partner AQRate Downshift Capability | 1 = Link Partner PHY supports AQRate fast-retrain downshift mechanism<br>0 = Link Partner PHY does *not* support AQRate fast-retrain downshift mechanism | R/W PD | 0 | |
| B | Link Partner 5G | 1 = Link Partner PHY is 5G capable<br>0 = Link Partner PHY is *not* 5G capable | R/W PD | 0 | |
| A | Link Partner 2.5G | 1 = Link Partner PHY is 5G capable<br>0 = Link Partner PHY is *not* 5G capable | R/W PD | 0 | |
| 9:3 | Reserved2 [6:0] | Reserved for future use | RO | | |
| 2 | Aquantia Link Partner | 1 = Link Partner is an Aquantia PHY<br>0 = Link Partner is *not* an Aquantia PHY | RO | | |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.79* **Autonegotiation Receive Link Partner Status 1: Address 7.E820**

### 6.9.80 Autonegotiation Receive Link Partner Status 2: Address 7.E821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.80* **Autonegotiation Receive Link Partner Status 2: Address 7.E821**

### 6.9.81 Autonegotiation Receive Link Partner Status 3: Address 7.E822

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.81* **Autonegotiation Receive Link Partner Status 3: Address 7.E822**

### 6.9.82 Autonegotiation Receive Link Partner Status 4: Address 7.E823

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Link Partner Firmware Major Revision Number [7:0] | [F:8] = Link partner firmware major revision number | RO | | Only the lower six bits of the major and minor firmware revision are exchanged in autonegotiation when the PHYID message is sent. Consequently, the upper 2 bits of the major and minor revision should always be zero. |
| 7:0 | Link Partner Firmware Minor Revision Number [7:0] | [7:0] = Link partner firmware minor revision number | RO | | |

*Table 6.9.82* **Autonegotiation Receive Link Partner Status 4: Address 7.E823**

### 6.9.83 Autonegotiation Receive Reserved Vendor Status 1: Address 7.E830

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Link Attempts [3:0] | Number of attempts needed to establish current link | RO<br>RW | | Once a link has been established, saves the total number of auto-negotiation and training sequence passes. |
| B:9 | Link Partner PHY Tag [2:0] | When the link partner is Aquantia and PHY ID pages have been exchanged, this field contains the vendor specific link partner PHY tag value | RO<br>RW | | This field is only valid if the link partner is Aquantia and PHY ID link pages have been exchanged during Autonegotiation. |
| 8:0 | Reserved Receive Status 1 [8:0] | Reserved for future use | RO | | |

*Table 6.9.83* **Autonegotiation Receive Reserved Vendor Status 1: Address 7.E830**

### 6.9.84 Autonegotiation Receive Reserved Vendor Status 2: Address 7.E831

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | Autonegotiation Protocol Error State | 1 = Link partner has violated the Autonegotiation protocol | RO | | This is the state bit associated with "Autonegotiation Protocol Error" (see “Autonegotiation Receive Vendor Alarms 2: Address 7.EC01” on page 415). |
| C | FLP Idle Error State | 1 = No FLP Burst has been seen for 50 milliseconds, forcing the receive state machine back to the Idle state | RO | | This is the state bit associated with "FLP Idle Error" (see “Autonegotiation Receive Vendor Alarms 2: Address 7.EC01” on page 415). |
| B:0 | Reserved Receive State 2 [B:0] | Reserved for future use | RO | | This is the state bit associated with "Reserved Receive Vendor Alarms 2 [B:0]" (see “Autonegotiation Receive Vendor Alarms 2: Address 7.EC01” on page 415). |

*Table 6.9.84* **Autonegotiation Receive Reserved Vendor Status 2: Address 7.E831**

### 6.9.85 Autonegotiation Receive Reserved Vendor Status 3: Address 7.E832

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved Receive State 3 [D:0] | Reserved for future use | RO | | |
| 1 | MultiGig Mode Selected | 1 = Indicates that MultiGig 2.5G or 5G mode was selected during autonegotiation process<br>0 = Indicates that MultiGig 2.5G or 5G mode was *not* selected. | RO | | Provides indication of whether the MultiGig mode 5G or 2.5G was selected during MDI autonegotiation process. |
| 0 | Link Partner AFR Enabled | 1 = The link partner has Aquantia Fast Reframe capability enabled | RO | | |

*Table 6.9.85* **Autonegotiation Receive Reserved Vendor Status 3: Address 7.E832**

### 6.9.86 Autonegotiation Receive Vendor Alarms 1: Address 7.EC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.86* **Autonegotiation Receive Vendor Alarms 1: Address 7.EC00**

### 6.9.87 Autonegotiation Receive Vendor Alarms 2: Address 7.EC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | Autonegotiation Protocol Error | 1 = Link partner has violated the Autonegotiation protocol | LH | | If the Arbiter state machine detects a protocol violation, the Autonegotiation process resets itself, and goes back to the “break link” state. |
| C | FLP Idle Error | 1 = No FLP Burst has been seen for 50 milliseconds, forcing the receive state machine back to the Idle state | LH | | Once FLP bursts are detected on any receive channel, they must keep coming. If no burst has been detected for a period of 50 milliseconds, the Autonegotiation process resets itself, and goes back to the “break link” state. |
| B:0 | Reserved Receive Vendor Alarms 2 [B:0] | Reserved for future use | LH | | |

*Table 6.9.87* **Autonegotiation Receive Vendor Alarms 2: Address 7.EC01**

### 6.9.88 Autonegotiation Receive Vendor Alarms 3: Address 7.EC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | 10BASE-T Device Detect | 0 = 10BASE-T device detected | LL | | Bit indicates that the detected far-end device is 10BASE-T when it is 0. This bit is 1 when link pulses are no longer received |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.88* **Autonegotiation Receive Vendor Alarms 3: Address 7.EC02**

### 6.9.89 Autonegotiation Receive Vendor Alarms 4: Address 7.EC03

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved Receive Vendor Alarms 4 [E:0] | Reserved | LH | | |
| 0 | 100BASE-TX Parallel Detect | 1 = 100BASE-TX parallel event detection occurred | LH | | |

*Table 6.9.89* **Autonegotiation Receive Vendor Alarms 4: Address 7.EC03**

### 6.9.90 Autonegotiation Receive Vendor Interrupt Mask 1: Address 7.F400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Receive Vendor Alarms 1 Mask [F:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0x0000 | |

*Table 6.9.90* **Autonegotiation Receive Vendor Interrupt Mask 1: Address 7.F400**

### 6.9.91 Autonegotiation Receive Vendor Interrupt Mask 2: Address 7.F401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | Autonegotiation Protocol Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | FLP Idle Error Mask | 1 = Enable interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0 | |
| B:0 | Reserved Receive Vendor Alarms 2 Mask [B:0] | 1 = Enable interrupt generation<br>0 = Disable interrupt generation | R/W PD | 0x000 | |

*Table 6.9.91* **Autonegotiation Receive Vendor Interrupt Mask 2: Address 7.F401**

### 6.9.92 Autonegotiation Receive Vendor Interrupt Mask 3: Address 7.F402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | 10BASE-T Device Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.92* **Autonegotiation Receive Vendor Interrupt Mask 3: Address 7.F402**

### 6.9.93 Autonegotiation Receive Vendor Interrupt Mask 4: Address 7.F403

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved Receive Vendor Alarms 4 Mask [E:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0x0000 | |
| 0 | 100BASE-TX Parallel Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.9.93* **Autonegotiation Receive Vendor Interrupt Mask 4: Address 7.F403**

### 6.9.94 Autonegotiation Vendor Global Interrupt Flags 1: Address 7.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Standard Alarms 1 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Standard Status 1: Address 7.1” on page 354) and the corresponding mask register (see “Autonegotiation Standard Interrupt Mask 1: Address 7.D000” on page 406). |
| E | Standard Alarms 2 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation 10GBASE-T Status Register: Address 7.21” on page 367) and the corresponding mask register (see “Autonegotiation Standard Interrupt Mask 2: Address 7.D001” on page 406). |
| D:B | Reserved | Internal reserved - do not modify | | | |

*Table 6.9.94* **Autonegotiation Vendor Global Interrupt Flags 1: Address 7.FC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A | Vendor Specific Alarms 1 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Transmit Vendor Alarms 1: Address 7.CC00” on page 404) and the corresponding mask register (see “Autonegotiation Transmit Vendor Interrupt Mask 1: Address 7.D400” on page 407). |
| 9 | Vendor Specific Alarms 2 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Transmit Vendor Alarms 2: Address 7.CC01” on page 405) and the corresponding mask register (see “Autonegotiation Transmit Vendor Interrupt Mask 2: Address 7.D401” on page 407). |
| 8:4 | Reserved | Internal reserved - do not modify | | | |
| 3 | Vendor Specific RX Alarms 1 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Receive Vendor Alarms 1: Address 7.EC00” on page 414) and the corresponding mask register (see “Autonegotiation Receive Vendor Interrupt Mask 1: Address 7.F400” on page 416). |
| 2 | Vendor Specific RX Alarms 2 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Receive Vendor Alarms 2: Address 7.EC01” on page 415) and the corresponding mask register (see “Autonegotiation Receive Vendor Interrupt Mask 2: Address 7.F401” on page 417). |

*Table 6.9.94* **Autonegotiation Vendor Global Interrupt Flags 1: Address 7.FC00** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | Vendor Specific RX Alarms 3 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Receive Vendor Alarms 3: Address 7.EC02” on page 415) and the corresponding mask register (see “Autonegotiation Receive Vendor Interrupt Mask 3: Address 7.F402” on page 417). |
| 0 | Vendor Specific RX Alarms 4 Interrupt | 1 = Interrupt | RO | | An interrupt was generated from status register (see “Autonegotiation Receive Vendor Alarms 4: Address 7.EC03” on page 416) and the corresponding mask register (see “Autonegotiation Receive Vendor Interrupt Mask 4: Address 7.F403” on page 418). |

*Table 6.9.94* **Autonegotiation Vendor Global Interrupt Flags 1: Address 7.FC00** (continued)

# 6.10 100BASE-TX and 1000BASE-T Registers

## 6.10.1 GbE Standard Device Identifier 1: Address 1D.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.10.1* **GbE Standard Device Identifier 1: Address 1D.2**

## 6.10.2 GbE Standard Device Identifier 2: Address 1D.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.10.2* **GbE Standard Device Identifier 2: Address 1D.3**

## 6.10.3 GbE Standard Devices in Package 1: Address 1D.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as there is Autonegotiation in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no MAC XAUI interface in the AQR107-AQR109. |

*Table 6.10.3* **GbE Standard Devices in Package 1: Address 1D.5**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | Control Present | 1 = Control is present in package<br>0 = Control is *not* present in package | ROS | 1 | Always set to 1, as there is a PHY XAUI interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1, as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1, as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.10.3* **GbE Standard Devices in Package 1: Address 1D.5** (continued)

### 6.10.4 GbE Standard Vendor Devices in Package 2: Address 1D.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the global control registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1 as the AQR107-AQR109 uses this device for the global control registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.4* **GbE Standard Vendor Devices in Package 2: Address 1D.6**

### 6.10.5 GbE Standard Status 2: Address 1D.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 2, as the Control is present in the AQR107-AQR109. |
| D:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.5* **GbE Standard Status 2: Address 1D.8**

### 6.10.6 GbE Standard Package Identifier 1: Address 1D.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31- 16 of Package ID | RO | | |

*Table 6.10.6* **GbE Standard Package Identifier 1: Address 1D.E**

### 6.10.7 GbE Standard Package Identifier 2: Address 1D.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15 - 0 of Package ID | RO | | |

*Table 6.10.7* **GbE Standard Package Identifier 2: Address 1D.F**

### 6.10.8 GbE PHY SGMII Test Control: Address 1D.C282

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.8* **GbE PHY SGMII Test Control: Address 1D.C282**

### 6.10.9 GbE PHY WoL Control 1: Address 1D.C300

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.9* **GbE PHY WoL Control 1: Address 1D.C300**

### 6.10.10 GbE PHY WoL Control 2: Address 1D.C301

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.10* **GbE PHY WoL Control 2: Address 1D.C301**

### 6.10.11 GbE PHY WoL Control 3: Address 1D.C302

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.11* **GbE PHY WoL Control 3: Address 1D.C302**

### 6.10.12 GbE PHY WoL Control 4: Address 1D.C303

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.12* **GbE PHY WoL Control 4: Address 1D.C303**

### 6.10.13 GbE PHY WoL Control 5: Address 1D.C304

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.13* **GbE PHY WoL Control 5: Address 1D.C304**

### 6.10.14 GbE PHY WoL Control 6: Address 1D.C305

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.14* **GbE PHY WoL Control 6: Address 1D.C305**

### 6.10.15 GbE PHY WoL Control 7: Address 1D.C306

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 0 [F:0] | Wake Up Frame Pattern Mask 0 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.15* **GbE PHY WoL Control 7: Address 1D.C306**

### 6.10.16 GbE PHY WoL Control 8: Address 1D.C307

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 1 [F:0] | Wake Up Frame Pattern Mask 0 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.16* **GbE PHY WoL Control 7: Address 1D.C306**

### 6.10.17 GbE PHY WoL Control 9: Address 1D.C308

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 2 [F:0] | Wake Up Frame Pattern Mask 0 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.17* **GbE PHY WoL Control 9: Address 1D.C308**

### 6.10.18 GbE PHY WoL Control 10: Address 1D.C309

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 3 [F:0] | Wake Up Frame Pattern Mask 0 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.18* **GbE PHY WoL Control 10: Address 1D.C309**

### 6.10.19 GbE PHY WoL Control 11: Address 1D.C30A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 4 [F:0] | Wake Up Frame Pattern Mask 0 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.19* **GbE PHY WoL Control 11: Address 1D.C30A**

### 6.10.20 GbE PHY WoL Control 12: Address 1D.C30B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 5 [F:0] | Wake Up Frame Pattern Mask 0 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.20* **GbE PHY WoL Control 12: Address 1D.C30B**

### 6.10.21 GbE PHY WoL Control 13: Address 1D.C30C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 6 [F:0] | Wake Up Frame Pattern Mask 0 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.21* **GbE PHY WoL Control 13: Address 1D.C30C**

### 6.10.22 GbE PHY WoL Control 14: Address 1D.C30D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 0 Word 7 [F:0] | Wake Up Frame Pattern Mask 0 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 0 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.22* **GbE PHY WoL Control 14: Address 1D.C30D**

### 6.10.23 GbE PHY WoL Control 15: Address 1D.C30E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 0 Word 0 [F:0] | Wake Up Frame CRC 0 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.23* **GbE PHY WoL Control 15: Address 1D.C30E**

### 6.10.24 GbE PHY WoL Control 16: Address 1D.C30F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 0 Word 1 [F:0] | Wake Up Frame CRC 0 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.24* **GbE PHY WoL Control 16: Address 1D.C30F**

### 6.10.25 GbE PHY WoL Control 17: Address 1D.C310

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 0 [F:0] | Wake Up Frame Pattern Mask 1 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.25* **GbE PHY WoL Control 17: Address 1D.C310**

### 6.10.26 GbE PHY WoL Control 18: Address 1D.C311

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 1 [F:0] | Wake Up Frame Pattern Mask 1 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.26* **GbE PHY WoL Control 18: Address 1D.C311**

### 6.10.27 GbE PHY WoL Control 19: Address 1D.C312

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 2 [F:0] | Wake Up Frame Pattern Mask 1 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.27* **GbE PHY WoL Control 19: Address 1D.C312**

### 6.10.28 GbE PHY WoL Control 20: Address 1D.C313

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 3 [F:0] | Wake Up Frame Pattern Mask 1 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.28* **GbE PHY WoL Control 20: Address 1D.C313**

### 6.10.29 GbE PHY WoL Control 21: Address 1D.C314

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 4 [F:0] | Wake Up Frame Pattern Mask 1 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.29* **GbE PHY WoL Control 21: Address 1D.C314**

### 6.10.30 GbE PHY WoL Control 22: Address 1D.C315

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 5 [F:0] | Wake Up Frame Pattern Mask 1 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.30* **GbE PHY WoL Control 22: Address 1D.C315**

### 6.10.31 GbE PHY WoL Control 23: Address 1D.C316

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 6 [F:0] | Wake Up Frame Pattern Mask 1 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.31* **GbE PHY WoL Control 23: Address 1D.C316**

### 6.10.32 GbE PHY WoL Control 24: Address 1D.C317

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 1 Word 7 [F:0] | Wake Up Frame Pattern Mask 1 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 1 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.32* **GbE PHY WoL Control 24: Address 1D.C317**

### 6.10.33 GbE PHY WoL Control 25: Address 1D.C318

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 1 Word 0 [F:0] | Wake Up Frame CRC 1 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.33* **GbE PHY WoL Control 25: Address 1D.C318**

### 6.10.34 GbE PHY WoL Control 26: Address 1D.C319

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 1 Word 1 [F:0] | Wake Up Frame CRC 1 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.34* **GbE PHY WoL Control 26: Address 1D.C319**

### 6.10.35 GbE PHY WoL Control 27: Address 1D.C31A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 0 [F:0] | Wake Up Frame Pattern Mask 2 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.35* **GbE PHY WoL Control 27: Address 1D.C31A**

### 6.10.36 GbE PHY WoL Control 28: Address 1D.C31B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 1 [F:0] | Wake Up Frame Pattern Mask 2 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.36* **GbE PHY WoL Control 28: Address 1D.C31B**

### 6.10.37 GbE PHY WoL Control 29: Address 1D.C31C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 2 [F:0] | Wake Up Frame Pattern Mask 2 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.37* **GbE PHY WoL Control 29: Address 1D.C31C**

### 6.10.38 GbE PHY WoL Control 30: Address 1D.C31D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 3 [F:0] | Wake Up Frame Pattern Mask 2 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.38* **GbE PHY WoL Control 30: Address 1D.C31D**

### 6.10.39 GbE PHY WoL Control 31: Address 1D.C31E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 4 [F:0] | Wake Up Frame Pattern Mask 2 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.39* **GbE PHY WoL Control 31: Address 1D.C31E**

### 6.10.40 GbE PHY WoL Control 32: Address 1D.C31F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 5 [F:0] | Wake Up Frame Pattern Mask 2 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.40* **GbE PHY WoL Control 32: Address 1D.C31F**

### 6.10.41 GbE PHY WoL Control 33: Address 1D.C320

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 6 [F:0] | Wake Up Frame Pattern Mask 2 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.41* **GbE PHY WoL Control 33: Address 1D.C320**

### 6.10.42 GbE PHY WoL Control 34: Address 1D.C321

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 2 Word 7 [F:0] | Wake Up Frame Pattern Mask 2 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 2 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.42* **GbE PHY WoL Control 34: Address 1D.C321**

### 6.10.43 GbE PHY WoL Control 35: Address 1D.C322

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 2 Word 0 [F:0] | Wake Up Frame CRC 2 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.43* **GbE PHY WoL Control 35: Address 1D.C322**

### 6.10.44 GbE PHY WoL Control 36: Address 1D.C323

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 2 Word 1 [F:0] | Wake Up Frame CRC 2 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.44* **GbE PHY WoL Control 36: Address 1D.C323**

### 6.10.45 GbE PHY WoL Control 37: Address 1D.C324

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 0 [F:0] | Wake Up Frame Pattern Mask 3 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.45* **GbE PHY WoL Control 37: Address 1D.C324**

### 6.10.46 GbE PHY WoL Control 38: Address 1D.C325

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 1 [F:0] | Wake Up Frame Pattern Mask 3 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.46* **GbE PHY WoL Control 38: Address 1D.C325**

### 6.10.47 GbE PHY WoL Control 39: Address 1D.C326

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 2 [F:0] | Wake Up Frame Pattern Mask 3 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.47* **GbE PHY WoL Control 39: Address 1D.C326**

### 6.10.48 GbE PHY WoL Control 40: Address 1D.C327

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 3 [F:0] | Wake Up Frame Pattern Mask 3 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.48* **GbE PHY WoL Control 40: Address 1D.C327**

### 6.10.49 GbE PHY WoL Control 41: Address 1D.C328

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 4 [F:0] | Wake Up Frame Pattern Mask 3 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.49* **GbE PHY WoL Control 41: Address 1D.C328**

### 6.10.50 GbE PHY WoL Control 42: Address 1D.C329

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 5 [F:0] | Wake Up Frame Pattern Mask 3 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.50* **GbE PHY WoL Control 42: Address 1D.C329**

### 6.10.51 GbE PHY WoL Control 43: Address 1D.C32A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 6 [F:0] | Wake Up Frame Pattern Mask 3 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.51* **GbE PHY WoL Control 43: Address 1D.C32A**

### 6.10.52 GbE PHY WoL Control 44: Address 1D.C32B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 3 Word 7 [F:0] | Wake Up Frame Pattern Mask 3 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 3 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.52* **GbE PHY WoL Control 44: Address 1D.C32B**

### 6.10.53 GbE PHY WoL Control 45: Address 1D.C32C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 3 Word 0 [F:0] | Wake Up Frame CRC 3 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.53* **GbE PHY WoL Control 45: Address 1D.C32C**

### 6.10.54 GbE PHY WoL Control 46: Address 1D.C32D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 3 Word 1 [F:0] | Wake Up Frame CRC 3 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.54* **GbE PHY WoL Control 46: Address 1D.C32D**

### 6.10.55 GbE PHY WoL Control 47: Address 1D.C32E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 0 [F:0] | Wake Up Frame Pattern Mask 4 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.55* **GbE PHY WoL Control 47: Address 1D.C32E**

### 6.10.56 GbE PHY WoL Control 48: Address 1D.C32F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 1 [F:0] | Wake Up Frame Pattern Mask 4 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.56* **GbE PHY WoL Control 48: Address 1D.C32F**

### 6.10.57 GbE PHY WoL Control 49: Address 1D.C330

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 2 [F:0] | Wake Up Frame Pattern Mask 4 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.57* **GbE PHY WoL Control 49: Address 1D.C330**

### 6.10.58 GbE PHY WoL Control 50: Address 1D.C331

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 3 [F:0] | Wake Up Frame Pattern Mask 4 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.58* **GbE PHY WoL Control 50: Address 1D.C331**

### 6.10.59 GbE PHY WoL Control 51: Address 1D.C332

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 4 [F:0] | Wake Up Frame Pattern Mask 4 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.59* **GbE PHY WoL Control 51: Address 1D.C332**

### 6.10.60 GbE PHY WoL Control 52: Address 1D.C333

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 5 [F:0] | Wake Up Frame Pattern Mask 4 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.60* **GbE PHY WoL Control 52: Address 1D.C333**

### 6.10.61 GbE PHY WoL Control 53: Address 1D.C334

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 6 [F:0] | Wake Up Frame Pattern Mask 4 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.61* **GbE PHY WoL Control 53: Address 1D.C334**

### 6.10.62 GbE PHY WoL Control 54: Address 1D.C335

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 4 Word 7 [F:0] | Wake Up Frame Pattern Mask 4 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 4 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.62* **GbE PHY WoL Control 54: Address 1D.C335**

### 6.10.63 GbE PHY WoL Control 55: Address 1D.C336

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 4 Word 0 [F:0] | Wake Up Frame CRC 4 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.63* **GbE PHY WoL Control 55: Address 1D.C336**

### 6.10.64 GbE PHY WoL Control 56: Address 1D.C337

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 4 Word 1 [F:0] | Wake Up Frame CRC 4 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.64* **GbE PHY WoL Control 56: Address 1D.C337**

### 6.10.65 GbE PHY WoL Control 57: Address 1D.C338

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.65* **GbE PHY WoL Control 57: Address 1D.C338**

### 6.10.66 GbE PHY WoL Control 58: Address 1D.C339

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Magic Packet Frame Pattern Word 0 [F:0] | Magic Packet Frame Pattern bits 15:0 | R/W | 0x0000 | Magic packet frame pattern (MAC address) |

*Table 6.10.66* **GbE PHY WoL Control 58: Address 1D.C339**

### 6.10.67 GbE PHY WoL Control 59: Address 1D.C33A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Magic Packet Frame Pattern Word 1 [F:0] | Magic Packet Frame Pattern bits 31:16 | R/W | 0x0000 | Magic packet frame pattern (MAC address) |

*Table 6.10.67* **GbE PHY WoL Control 59: Address 1D.C33A**

### 6.10.68 GbE PHY WoL Control 60: Address 1D.C33B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Magic Packet Frame Pattern Word 2 [F:0] | Magic Packet Frame Pattern bits 47:32 | R/W | 0x0000 | Magic packet frame pattern (MAC address) |

*Table 6.10.68* **GbE PHY WoL Control 60: Address 1D.C33B**

### 6.10.69 GbE PHY Extended WoL Control 1: Address 1D.C420

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 0 [F:0] | Wake Up Frame Pattern Mask 5 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.69* **GbE PHY Extended WoL Control 1: Address 1D.C420**

### 6.10.70 GbE PHY Extended WoL Control 2: Address 1D.C421

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 1 [F:0] | Wake Up Frame Pattern Mask 55 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.70* **GbE PHY Extended WoL Control 2: Address 1D.C421**

### 6.10.71 GbE PHY Extended WoL Control 3: Address 1D.C422

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 2 [F:0] | Wake Up Frame Pattern Mask 5 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.71* **GbE PHY Extended WoL Control 3: Address 1D.C422**

### 6.10.72 GbE PHY Extended WoL Control 4: Address 1D.C423

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 3 [F:0] | Wake Up Frame Pattern Mask 5 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.72* **GbE PHY Extended WoL Control 4: Address 1D.C423**

### 6.10.73 GbE PHY Extended WoL Control 5: Address 1D.C424

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 4 [F:0] | Wake Up Frame Pattern Mask 5 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.73* **GbE PHY Extended WoL Control 5: Address 1D.C424**

### 6.10.74 GbE PHY Extended WoL Control 6: Address 1D.C425

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 5 [F:0] | Wake Up Frame Pattern Mask 5 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.74* **GbE PHY Extended WoL Control 6: Address 1D.C425**

### 6.10.75 GbE PHY Extended WoL Control 7: Address 1D.C426

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 6 [F:0] | Wake Up Frame Pattern Mask 5 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.75* **GbE PHY Extended WoL Control 7: Address 1D.C426**

### 6.10.76 GbE PHY Extended WoL Control 8: Address 1D.C427

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 5 Word 7 [F:0] | Wake Up Frame Pattern Mask 5 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 5 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.76* **GbE PHY Extended WoL Control 8: Address 1D.C427**

### 6.10.77 GbE PHY Extended WoL Control 9: Address 1D.C428

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 5 Word 0 [F:0] | Wake Up Frame CRC 5 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.77* **GbE PHY Extended WoL Control 9: Address 1D.C428**

### 6.10.78 GbE PHY Extended WoL Control 10: Address 1D.C429

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 5 Word 1 [F:0] | Wake Up Frame CRC 5 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.78* **GbE PHY Extended WoL Control 10: Address 1D.C429**

### 6.10.79 GbE PHY Extended WoL Control 11: Address 1D.C42A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 0 [F:0] | Wake Up Frame Pattern Mask 6 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte; default: all-zeros). |

*Table 6.10.79* **GbE PHY Extended WoL Control 11: Address 1D.C42A**

### 6.10.80 GbE PHY Extended WoL Control 12: Address 1D.C42B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 1 [F:0] | Wake Up Frame Pattern Mask 65 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.80* **GbE PHY Extended WoL Control 12: Address 1D.C42B**

### 6.10.81 GbE PHY Extended WoL Control 13: Address 1D.C42C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 2 [F:0] | Wake Up Frame Pattern Mask 6 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.81* **GbE PHY Extended WoL Control 13: Address 1D.C42C**

### 6.10.82 GbE PHY Extended WoL Control 14: Address 1D.C42D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 3 [F:0] | Wake Up Frame Pattern Mask 6 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.82* **GbE PHY Extended WoL Control 14: Address 1D.C42D**

### 6.10.83 GbE PHY Extended WoL Control 15: Address 1D.C42E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 4 [F:0] | Wake Up Frame Pattern Mask 6 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.83* **GbE PHY Extended WoL Control 15: Address 1D.C42E**

### 6.10.84 GbE PHY Extended WoL Control 16: Address 1D.C42F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 5 [F:0] | Wake Up Frame Pattern Mask 6 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.84* **GbE PHY Extended WoL Control 16: Address 1D.C42F**

### 6.10.85 GbE PHY Extended WoL Control 17: Address 1D.C430

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 6 [F:0] | Wake Up Frame Pattern Mask 6 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.85* **GbE PHY Extended WoL Control 17: Address 1D.C430**

### 6.10.86 GbE PHY Extended WoL Control 18: Address 1D.C431

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 6 Word 7 [F:0] | Wake Up Frame Pattern Mask 6 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 6 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.86* **GbE PHY Extended WoL Control 18: Address 1D.C431**

### 6.10.87 GbE PHY Extended WoL Control 19: Address 1D.C432

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 6 Word 0 [F:0] | Wake Up Frame CRC 6 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.87* **GbE PHY Extended WoL Control 19: Address 1D.C432**

### 6.10.88 GbE PHY Extended WoL Control 20: Address 1D.C433

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 6 Word 1 [F:0] | Wake Up Frame CRC 6 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.88* **GbE PHY Extended WoL Control 20: Address 1D.C433**

### 6.10.89 GbE PHY Extended WoL Control 21: Address 1D.C434

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 0 [F:0] | Wake Up Frame Pattern Mask 7 bits 15:0 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.89* **GbE PHY Extended WoL Control 21: Address 1D.C434**

### 6.10.90 GbE PHY Extended WoL Control 22: Address 1D.C435

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 1 [F:0] | Wake Up Frame Pattern Mask 75 bits 31:16 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.90* **GbE PHY Extended WoL Control 22: Address 1D.C435**

### 6.10.91 GbE PHY Extended WoL Control 23: Address 1D.C436

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 2 [F:0] | Wake Up Frame Pattern Mask 7 bits 47:32 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.91* **GbE PHY Extended WoL Control 23: Address 1D.C436**

### 6.10.92 GbE PHY Extended WoL Control 24: Address 1D.C437

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 3 [F:0] | Wake Up Frame Pattern Mask 7 bits 63:48 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.92* **GbE PHY Extended WoL Control 24: Address 1D.C437**

### 6.10.93 GbE PHY Extended WoL Control 25: Address 1D.C438

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 4 [F:0] | Wake Up Frame Pattern Mask 7 bits 79:64 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.93* **GbE PHY Extended WoL Control 25: Address 1D.C438**

### 6.10.94 GbE PHY Extended WoL Control 26: Address 1D.C439

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 5 [F:0] | Wake Up Frame Pattern Mask 7 bits 95:80 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.94* **GbE PHY Extended WoL Control 26: Address 1D.C439**

### 6.10.95 GbE PHY Extended WoL Control 27: Address 1D.C43A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 6 [F:0] | Wake Up Frame Pattern Mask 7 bits 111:96 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.95* **GbE PHY Extended WoL Control 27: Address 1D.C43A**

### 6.10.96 GbE PHY Extended WoL Control 28: Address 1D.C43B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame Mask 7 Word 7 [F:0] | Wake Up Frame Pattern Mask 7 bits 127:112 | R/W | 0x0000 | Wake-up Frame Pattern Mask 7 (0 = disable, 1 = enable, bit 0 for the first byte, default: all-zeros). |

*Table 6.10.96* **GbE PHY Extended WoL Control 28: Address 1D.C43B**

### 6.10.97 GbE PHY Extended WoL Control 29: Address 1D.C43C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 7 Word 0 [F:0] | Wake Up Frame CRC 7 bits 15:0 | R/W | 0x0000 | |

*Table 6.10.97* **GbE PHY Extended WoL Control 29: Address 1D.C43C**

### 6.10.98 GbE PHY Extended WoL Control 30: Address 1D.C43D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Wake Up Frame CRC 7 Word 1 [F:0] | Wake Up Frame CRC 7 bits 31:16 | R/W | 0x0000 | |

*Table 6.10.98* **GbE PHY Extended WoL Control 30: Address 1D.C43D**

### 6.10.99 GbE Reserved Provisioning 1: Address 1D.C500

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | 100M System Loopback | 1 = Enables System Loopback | R/W PD | 0 | Setting this bit enables the 100M system loopback.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| E | GbE System Loopback | 1 = Enables System Loopback | R/W PD | 0 | Setting this bit enables the 1G system loopback.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| D:0 | Reserved Provisioning 1 [D:0] | Reserved for future use | R/W PD | 0x0000 | |

*Table 6.10.99* **GbE Reserved Provisioning 1: Address 1D.C500**

### 6.10.100 GbE Reserved Provisioning 2: Address 1D.C501

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Test Mode [2:0] | 000 = Normal mode<br>001 = Test Mode 1 - Transmit waveform test<br>010 = Test Mode 2 - Master transmit jitter test<br>011 = Test Mode 3 - Slave transmit jitter test<br>100 = Test Mode 4 - Transmitter distortion test<br>101 -> 1111 = Reserved | R/W | 0x0 | **Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |
| C:2 | Reserved Provisioning 2 [A:0] | Reserved for future use | R/W PD | 0x000 | |
| 1:0 | 100BASE-TX Test Mode [1:0] | 00 = Normal mode<br>01 = 100BASE-TX IEEE Test Mode<br>10 = 100BASE-TX ANSI Jitter Test<br>11 = 100BASE-TX ANSI Droop Test | R/W | 0x0 | 100BASE-TX IEEE Test Mode = MLT-3 Idle Sequence<br>ANSI Jitter Test = FDDI - Clause 9.1.3 Fig. 12<br>ANSI Droop Test = FDDI - Clause 9.1.8 Fig. 14<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F. |

*Table 6.10.100* **GbE Reserved Provisioning 2: Address 1D.C501**

### 6.10.101 GbE PHY TGE Status 3: 1D.D202

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | TGE EEE RX LPI Received | 1 = RX LPI has been detected | BLH | | Indicates that RX LPI has been detected. |
| 4 | TGE EEE RX LPI Indication | 1 = RX LPI is currently detected | RO | | Indicates that RX LPI is currently detected. |
| 3 | TGE EEE RX LPI Wake Timer Fault Error | 1 = RX LPI detected Wake Timer fault | BLH | | Indicates that RX LPI detected a Wake Timer fault. |
| 2 | TGE EEE RX LPI Link Fail Timer Done | 1 = RX LPI Link Fail Timer Done | BLH | | Indicates that RX LPI detected a Link Fail Timer done. |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.101* **GbE PHY TGE Status 3: 1D.D202**

### 6.10.102 GbE PHY TGE Status 4: 1D.D203

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | TGE EEE TX LPI Received | 1 = TX LPI has been detected | BLH | | Indicates that TX LPI has been detected. |
| 4 | TGE EEE TX LPI Indication | 1 = TX LPI is currently detected | RO | | Indicates that TX LPI is currently detected. |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.102* **GbE PHY TGE Status 4: 1D.D203**

### 6.10.103 GbE PHY SGMII1 RX Status 1: Address 1D.D280

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.103* **GbE PHY SGMII 1**

### 6.10.104 GbE PHY SGMII1 RX Status 2: Address 1D.D281

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.104* **GbE PHY SGMII1 RX Status 2: Address 1D.D281**

### 6.10.105 GbE PHY SGMII1 RX Status 3: Address 1D.D282

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.105* **GbE PHY SGMII1 RX Status 3: Address 1D.D282**

### 6.10.106 GbE PHY SGMII1 RX Status 4: Address 1D.D283

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.106* **GbE PHY SGMII1 RX Status 4: Address 1D.D283**

### 6.10.107 GbE PHY SGMII1 RX Status 5: Address 1D.D284

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.107* **GbE PHY SGMII1 RX Status 5: Address 1D.D284**

### 6.10.108 GbE PHY SGMII1 RX Status 6: Address 1D.D285

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.108* **GbE PHY SGMII1 RX Status 6: Address 1D.D285**

### 6.10.109 GbE PHY SGMII1 RX Status 7: Address 1D.D286

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.109* **GbE PHY SGMII1 RX Status 7: Address 1D.D286**

### 6.10.110 GbE PHY SGMII1 RX Status 8: Address 1D.D287

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.110* **GbE PHY SGMII1 RX Status 8: Address 1D.D287**

### 6.10.111 GbE PHY SGMII1 RX Status 9: Address 1D.D288

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.111* **GbE PHY SGMII1 RX Status 9: Address 1D.D288**

### 6.10.112 GbE PHY SGMII0 RX Status 1: Address 1D.D290

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:9 | Reserved | Internal reserved - do not modify | | | |
| 8 | SGMII0 RX Synchronization Status | 1 = SGMII0 RX is Synchronized | RO | | |

*Table 6.10.112* **GbE PHY SGMII0 RX Status 1: Address 1D.D290**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | SGMII0 RX Loopback Idle Insertion Detected | 1 = SGMII0 RX Idle Insertion Detected | LH | | |
| 6 | SGMII0 RX Loopback Idle Deletion Detected | 1 = SGMII0 RX Idle Deletion Detected | LH | | |
| 5 | SGMII0 RX Idle Insertion Detected | 1 = SGMII0 RX Idle Insertion Detected | LH | | |
| 4 | SGMII0 RX Idle Deletion Detected | 1 = SGMII0 RX Idle Deletion Detected | LH | | |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | SGMII0 RX TX_ER Suppression | 1 = SGMII0 RX TX_ER suppressed | LH | | Indicates that TX_ER has been suppressed when TX_EN was *not* asserted. |
| 0 | SGMII0 RX RX Link Activity | 1 = SGMII0 RX RX Link Activity | LH | | Indicates that SGMII Start Character K27_7 is detected. |

*Table 6.10.112* **GbE PHY SGMII0 RX Status 1: Address 1D.D290** (continued)

### 6.10.113 GbE PHY SGMII0 RX Status 2: Address 1D.D291

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.113* **GbE PHY SGMII0 RX Status 2: Address 1D.D291**

### 6.10.114 GbE PHY SGMII0 RX Status 3: Address 1D.D292

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 RX Frame Counter LSW [F:0] | SGMII0 RX Good Frame Counter | SCTL | 0x0000 | This counts the 100M/GbE Ethernet good frames (for example, those with no Ethernet CRC-32/FCS errors). |

*Table 6.10.114* **GbE PHY SGMII0 RX Status 3: Address 1D.D292**

### 6.10.115 GbE PHY SGMII0 RX Status 4: Address 1D.D293

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | SGMII0 RX Frame Counter MSW [9:0] | SGMII0 RX Good Frame Counter | SCTM | 0x000 | Counts 100M/GbE Ethernet good frames (for example, those with no Ethernet CRC-32/FCS errors). |

*Table 6.10.115* **GbE PHY SGMII0 RX Status 4: Address 1D.D293**

### 6.10.116 GbE PHY SGMII0 RX Status 5: Address 1D.D294

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 RX Frame Error Counter LSW [F:0] | SGMII0 RX Bad Frame Counter | SCTL | 0x0000 | This counts 100M/GbE Ethernet frames with a bad FCS (also known as CRC-32). |

*Table 6.10.116* **GbE PHY SGMII0 RX Status 5: Address 1D.D294**

### 6.10.117 GbE PHY SGMII0 RX Status 6: Address 1D.D295

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | SGMII0 RX Frame Error Counter MSW [9:0] | SGMII0 RX Bad Frame Counter | SCTM | 0x000 | This counts 100M/GbE Ethernet frames with a bad FCS (also known as CRC-32). |

*Table 6.10.117* **GbE PHY SGMII0 RX Status 6: Address 1D.D295**

### 6.10.118 GbE PHY SGMII0 RX Status 7: Address 1D.D296

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | SGMII0 RX Comma Detect | 1 = SGMII0 RX Comma Detected | LH | | Indicates when RX has detected a comma character |

*Table 6.10.118* **GbE PHY SGMII0 RX Status 7: Address 1D.D296**

### 6.10.119 GbE PHY SGMII0 RX Status 8: Address 1D.D297

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | SGMII0 RX False Carrier Counter [7:0] | SGMII0 RX False Carrier Counter | SCT | 0x00 | False carrier events on XFI0 SGMII interface. |

*Table 6.10.119* **GbE PHY SGMII0 RX Status 8: Address 1D.D297**

### 6.10.120 GbE PHY SGMII0 RX Status 9: Address 1D.D298

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:C | Reserved | Internal reserved - do not modify | | | |
| B:8 | SGMII0 RX EEE RX LPI State Machine [3:0] | SGMII0 RX EEE RX LPI state machine | RO | | Indicates the RX LPI state machine. |
| 7:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | SGMII0 RX EEE RX LPI Ordered Set Detected | 1 = SGMII0 RX LPI ordered set detected | LH | | Indicates that the LPI ordered_set is detected. |
| 3 | SGMII0 RX EEE RX LPI Wake Timer Fault Error | 1 = SGMII0 RX RX LPI detected wake timer fault | LH | | Indicates a RX LPI detected wake timer fault. |
| 2 | SGMII0 RX EEE RX LPI Wake Done State | 1 = SGMII0 RX RX LPI is in wake done state | RO | | Indicates that RX LPI is in a wake done state. |
| 1 | SGMII0 RX EEE RX LPI Quiet State | 1 = SGMII0 RX RX LPI is in quiet state | RO | | Indicates that RX LPI is in a quiet state. |
| 0 | SGMII0 RX EEE RX LPI Active State | 1 = SGMII0 RX RX LPI is in active state | RO | | Indicates that RX LPI is in an active state. |

*Table 6.10.120* **GbE PHY SGMII0 RX Status 9: Address 1D.D298**

### 6.10.121 GbE PHY SGMII1 WoL Status: Address 1D.D302

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.121* **GbE PHY SGMII1 WoL Status: Address 1D.D302**

### 6.10.122 GbE PHY SGMII1 TX Status 1: Address 1D.D303

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.122* **GbE PHY SGMII1 RX Status 3: Address 1D.D282**

### 6.10.123 GbE PHY SGMII1 TX Status 2: Address 1D.D304

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.123* **GbE PHY SGMII1 RX Status 4: Address 1D.D283**

### 6.10.124 GbE PHY SGMII1 TX Status 3: Address 1D.D305

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.124* **GbE PHY SGMII1 RX Status 5: Address 1D.D284**

### 6.10.125 GbE PHY SGMII1 TX Status 4: Address 1D.D306

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.125* **GbE PHY SGMII1 RX Status 6: Address 1D.D285**

### 6.10.126 GbE PHY SGMII1 TX Status 5: Address 1D.D307

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.126* **GbE PHY SGMII1 TX Status 5: Address 1D.D307**

### 6.10.127 GbE PHY SGMII1 TX Status 6: Address 1D.D308

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.127* **GbE PHY SGMII1 TX Status 6: Address 1D.D308**

### 6.10.128 GbE PHY SGMII1 TX Status 7: Address 1D.D309

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.128* **GbE PHY SGMII1 TX Status 7: Address 1D.D309**

### 6.10.129 GbE PHY SGMII1 TX Status 8: Address 1D.D30A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.129* **GbE PHY SGMII1 TX Status 8: Address 1D.D30A**

### 6.10.130 GbE PHY SGMII1 TX Status 9: Address 1D.D30B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.130* **GbE PHY SGMII1 TX Status 9: Address 1D.D30B**

### 6.10.131 GbE PHY SGMII1 TX Status 10: Address 1D.D30C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.131* **GbE PHY SGMII1 TX Status 10: Address 1D.D30C**

### 6.10.132 SGMII0 WoL Status: Address 1D.D312

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | SGMII0 Wake Up Frame Type [2:0] | SGMII0 Wake Up Frame Type | RO | | Wake-up Frame type detected (0 to 7: Wake-up Frame, 0 to 7). |

*Table 6.10.132* **SGMII0 WoL Status: Address 1D.D312**

### 6.10.133 GbE PHY SGMII0 TX Status 1: Address 1D.D313

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 TX Frame Counter LSW [F:0] | SGMII0 TX Good Frame Counter | SCTL | 0x0000 | This counts 100M/GbE Ethernet good frames (for example, those with no Ethernet CRC-32/FCS errors). |

*Table 6.10.133* **GbE PHY SGMII0 TX Status 1: Address 1D.D313**

### 6.10.134 GbE PHY SGMII0 TX Status 2: Address 1D.D314

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | SGMII0 TX Frame Counter MSW [9:0] | SGMII0 TX Good Frame Counter | SCTM | 0x000 | This counts 100M/GbE Ethernet good frames (for example, those with no Ethernet CRC-32/FCS errors). |

*Table 6.10.134* **GbE PHY SGMII0 TX Status 2: Address 1D.D314**

### 6.10.135 GbE PHY SGMII0 TX Status 3: Address 1D.D315

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 TX Frame Error Counter LSW [F:0] | SGMII0 TX Bad Frame Error Counter | SCTL | 0x0000 | This counts 100M/GbE Ethernet frames with a bad FCS (also known as CRC-32). |

*Table 6.10.135* **GbE PHY SGMII0 TX Status 3: Address 1D.D315**

### 6.10.136 GbE PHY SGMII0 TX Status 4: Address 1D.D316

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:0 | SGMII0 TX Frame Error Counter MSW [9:0] | SGMII0 TX Bad Frame Error Counter | SCTM | 0x000 | This counts 100M/GbE Ethernet frames with a bad FCS (also known as CRC-32). |

*Table 6.10.136* **GbE PHY SGMII0 TX Status 4: Address 1D.D316**

### 6.10.137 GbE PHY SGMII0 TX Status 5: Address 1D.D317

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | SGMII0 TX False Carrier Counter [7:0] | SGMII0 TX False Carrier Counter | SCT | 0x00 | SGMII0 TX detected a false carrier on the GMII/MII interface. |

*Table 6.10.137* **GbE PHY SGMII0 TX Status 5: Address 1D.D317**

### 6.10.138 GbE PHY SGMII0 TX Status 6: Address 1D.D318

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | SGMII0 TX Collision Counter [7:0] | SGMII0 TX Collision Counter | SCT | 0x00 | SGMII0 TX detected a collision on the SGMII interface. |

*Table 6.10.138* **GbE PHY SGMII0 TX Status 6: Address 1D.D318**

### 6.10.139 GbE PHY SGMII0 TX Status 7: Address 1D.D319

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | SGMII0 TX Line Collision Counter [7:0] | SGMII0 TX Line Collision Counter | SCT | 0x00 | SGMII0 TX detected a collision on the GMII/MII interface. |

*Table 6.10.139* **GbE PHY SGMII0 TX Status 7: Address 1D.D319**

### 6.10.140 GbE PHY SGMII0 TX Status 8: Address 1D.D31A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 TX Frame Alignment Counter [F:0] | SGMII0 TX Frame Alignment Counter | SCT | 0x0000 | SGMII0 TX Frame Count with an alignment error. This is detected by CRC error with an extra nibble on the MII interface (100M mode) on the GMII/MII interface. |

*Table 6.10.140* **GbE PHY SGMII0 TX Status 8: Address 1D.D31A**

### 6.10.141 GbE PHY SGMII0 TX Status 9: Address 1D.D31B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | SGMII0 TX Runt Frame Counter LSW [F:0] | SGMII0 TX Runt Frame Counter | SCTL | 0x0000 | SGMII0 TX Runt Frame Count (less than 64 bytes long) on the GMII/MII interface. |

*Table 6.10.141* **GbE PHY SGMII0 TX Status 9: Address 1D.D31B**

### 6.10.142 GbE PHY SGMII0 TX Status 10: Address 1D.D31C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | SGMII0 TX Runt Frame Counter MSW [5:0] | SGMII0 TX Runt Frame Counter | SCTM | 0x00 | SGMII0 TX Runt Frame Count (less than 64 bytes long) on the GMII/MII interface. |

*Table 6.10.142* **GbE PHY SGMII0 TX Status 10: Address 1D.D31C**

### 6.10.143 GbE PHY SGMII WoL Status: Address 1D.D322

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.143* **GbE PHY SGMII WoL Status: Address 1D.D322**

### 6.10.144 GbE PHY SGMII RX Alarms 1: Address 1D.EC10

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | SGMII0 RX Loss of Signal | 1 = SGMII0 Loss of Signal | LH | | |
| 6 | SGMII0 RX Invalid Character Error | 1 = SGMII0 RX Invalid Character Error | LH | | |
| 5 | SGMII0 RX Running Disparity Error | 1 = SGMII0 RX Running Disparity Error | LH | | |
| 4 | SGMII0 RX Code Violation Error | 1 = SGMII0 RX Code Violation Error | LH | | |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.144* **GbE PHY SGMII RX Alarms 1: Address 1D.EC10**

### 6.10.145 GbE PHY SGMII TX Alarms 1: Address 1D.EC20

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | SGMII0 TX Invalid GMII Character Detected | 1 = SGMII0 TX Invalid GMII Character Detected | LH | | |
| 5 | SGMII0 Magic Packet Frame Detected | 1 = SGMII0 Magic Packet Frame Detected | LH | | |
| 4 | SGMII0 Wake Up Frame Detected | 1 = SGMII0 Wake Up Frame Detected | LH | | |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.145* **GbE PHY SGMII TX Alarms 1: Address 1D.EC20**

### 6.10.146 GbE PHY SGMII RX Interrupt Mask 1: Address 1D.F410

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | SGMII0 RX Loss of Signal Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 6 | SGMII0 RX Invalid Character Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 5 | SGMII0 RX Running Disparity Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 4 | SGMII0 RX Code Violation Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.146* **GbE PHY SGMII RX Interrupt Mask 1: Address 1D.F410**

### 6.10.147 GbE PHY SGMII TX Interrupt Mask 1: Address 1D.F420

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | SGMII0 TX Invalid GMII Character Detected Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 5 | SGMII0 Magic Packet Frame Detected Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 4 | SGMII0 Wake Up Frame Detected Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.147* **GbE PHY SGMII TX Interrupt Mask 1: Address 1D.F420**

### 6.10.148 GbE PHY Vendor Global Interrupt Flags 1: Address 1D.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | Vendor Specific SGMII TX Alarms 1 Interrupt | 1 = Interrupt in vendor-specific SGMII TX Alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 3 | Vendor Specific SGMII TX Alarms 2 Interrupt | 1 = Interrupt in vendor-specific SGMII TX Alarms 2 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 2 | Vendor Specific SGMII RX Alarms 1 Interrupt | 1 = Interrupt in vendor-specific SGMII TX Alarms 1 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 1 | Vendor Specific SGMII RX Alarms 2 Interrupt | 1 = Interrupt in vendor-specific SGMII TX Alarms 2 | RO | | An interrupt was generated from the status register and the corresponding mask register. |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.10.148* **GbE PHY Vendor Global Interrupt Flags 1: Address 1D.FC00**

# 6.11 Global Registers

## 6.11.1 Global Standard Control 1: Address 1E.0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Soft Reset | 1 = Global soft reset<br>0 = Normal operation | R/W SC | 1 | Resets the entire PHY. Setting this bit initiates a global soft reset on all of the digital logic except for the microprocessor (the microprocessor is *not* reset). Upon completion of the reset sequence, this bit is set back to 0 by the microprocessor. Note this bit is OR'ed with the individual MMD resets.<br><br>**Note:** This bit should be set to 0 before setting the individual MMD resets. |
| E:C | Reserved | Internal reserved - do not modify | | | |
| B | Low Power | 1 = Low-power mode<br>0 = Normal operation | R/W PD | 0 | A 1 written to this register causes the chip to enter low-power mode, and this bit puts the entire chip in low-power mode, with only the MDIO and microprocessor functioning, and turns off the analog front-end (for example, it places it in high-impedance mode). Setting this bit also sets all of the Low Power bits in the other MMDs. |
| A:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.1* **Global Standard Control 1: Address 1E.0**

## 6.11.2 Global Standard Device Identifier 1: Address 1E.2

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID MSW [1F:10] | Bits 31 - 16 of Device ID | RO | | |

*Table 6.11.2* **Global Standard Device Identifier 1: Address 1E.2**

### 6.11.3 Global Standard Device Identifier 2: Address 1E.3

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Device ID LSW [F:0] | Bits 15 - 0 of Device ID | RO | | |

*Table 6.11.3* **Global Standard Device Identifier 2: Address 1E.3**

### 6.11.4 Global Standard Devices in Package 1: Address 1E.5

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Autonegotiation Present | 1 = Autonegotiation is present in package<br>0 = Autonegotiation is *not* present in package | ROS | 1 | Always set to 1, as there is Autonegotiation in the AQR107-AQR109. |
| 6 | TC Present | 1 = TC is present in package<br>0 = TC is *not* present in package | ROS | 0 | Always set to 0, as there is no TC functionality in the AQR107-AQR109. |
| 5 | DTE XS Present | 1 = DTE XS is present in package<br>0 = DTE XS is *not* present in package | ROS | 0 | Always set to 0, as there is no DTE XAUI interface in the AQR107-AQR109. |
| 4 | PHY XS Present | 1 = PHY XS is present in package<br>0 = PHY XS is *not* present in package | ROS | 1 | Always set to 1, as there is a PHY XS interface in the AQR107-AQR109. |
| 3 | PCS Present | 1 = PCS is present in package<br>0 = PCS is *not* present in package | ROS | 1 | Always set to 1, as there is PCS functionality in the AQR107-AQR109. |
| 2 | WIS Present | 1 = WIS is present in package<br>0 = WIS is *not* present in package | ROS | 0 | Always set to 0, as there is no WIS functionality in the AQR107-AQR109. |

*Table 6.11.4* **Global Standard Devices in Package 1: Address 1E.5**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | PMA Present | 1 = PMA is present in package<br>0 = PMA is *not* present | ROS | 1 | Always set to 1, as there is PMA functionality in the AQR107-AQR109. |
| 0 | Clause 22 Registers Present | 1 = Clause 22 registers are present in package<br>0 = Clause 22 registers are *not* present in package | ROS | 0 | Always set to 0 in the AQR107-AQR109, as there are no Clause 22 registers in the device. |

*Table 6.11.4* **Global Standard Devices in Package 1: Address 1E.5** (continued)

### 6.11.5 Global Standard Vendor Devices in Package 2: Address 1E.6

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Vendor Specific Device #2 Present | 1 = Device #2 is present in package<br>0 = Device #2 is *not* present in package | ROS | 1 | Always set to 1, as the AQR107-AQR109 uses this device for the DSP PMA registers. |
| E | Vendor Specific Device #1 Present | 1 = Device #1 is present in package<br>0 = Device #1 is *not* present in package | ROS | 1 | Always set to 1, as the AQR107-AQR109 uses this device for the global control registers. |
| D | Clause 22 Extension Present | 1 = Clause 22 Extension is present in package<br>0 = Clause 22 Extension is *not* present in package | ROS | 1 | Always set to 1, as the AQR107-AQR109 uses this device for the GbE registers. |
| C:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.5* **Global Standard Vendor Devices in Package 2: Address 1E.6**

### 6.11.6 Global Standard Status 2: Address 1E.8

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Device Present [1:0] | [F:E]<br>0x3 = No device at this address<br>0x2 = Device present at this address<br>0x1 = No device at this address<br>0x0 = No device at this address | ROS | 0x2 | Field is always set to 0x2, as the Global MMD resides here in the AQR107-AQR109. |
| D:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.6* **Global Standard Status 2: Address 1E.8**

### 6.11.7 Global Standard Package Identifier 1: Address 1E.E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID MSW [1F:10] | Bits 31- 16 of Package ID | RO | | |

*Table 6.11.7* **Global Standard Package Identifier 1: Address 1E.E**

### 6.11.8 Global Standard Package Identifier 2: Address 1E.F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Package ID LSW [F:0] | Bits 15 - 0 of Package ID | RO | | |

*Table 6.11.8* **Global Standard Package Identifier 2: Address 1E.F**

### 6.11.9 Global Firmware ID: Address 1E.20

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Firmware Major Revision Number [7:0] | [F:8] = Major revision number | RO | | The lower six bits of major and minor firmware revision are exchanged in autonegotiation when the PHYID message is sent. |
| 7:0 | Firmware Minor Revision Number [7:0] | [7:0] = Minor revision number | RO | | |

*Table 6.11.9* **Global Firmware ID: Address 1E.20**

### 6.11.10 Global Programmable MMD Register 1: Address 1E.80

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 0 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 0 [A:0] | Remapped MMD Address | R/W | 0x318 | Indicates the global register address to remap. |

*Table 6.11.10* **Global Programmable MMD Register 1: Address 1E.80**

### 6.11.11 Global Programmable MMD Register 2: Address 1E.81

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 0 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.11* **Global Programmable MMD Register 2: Address 1E.81**

### 6.11.12 Global Programmable MMD Register 3: Address 1E.82

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 1 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 1 [A:0] | Remapped MMD Address | R/W | 0x319 | Indicates the global register address to remap. |

*Table 6.11.12* **Global Programmable MMD Register 3: Address 1E.82**

### 6.11.13 Global Programmable MMD Register 4: Address 1E.83

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 1 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.13* **Global Programmable MMD Register 4: Address 1E.83**

### 6.11.14 Global Programmable MMD Register 5: Address 1E.84

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 2 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 2 [A:0] | Remapped MMD Address | R/W | 0x31A | Indicates the global register address to remap. |

*Table 6.11.14* **Global Programmable MMD Register 5: Address 1E.84**

### 6.11.15 Global Programmable MMD Register 6: Address 1E.85

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 2 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.15* **Global Programmable MMD Register 6: Address 1E.85**

### 6.11.16 Global Programmable MMD Register 7: Address 1E.86

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 3 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 3 [A:0] | Remapped MMD Address | R/W | 0x31B | Indicates the global register address to remap. |

*Table 6.11.16* **Global Programmable MMD Register 7: Address 1E.86**

### 6.11.17 Global Programmable MMD Register 8: Address 1E.87

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 3 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.17* **Global Programmable MMD Register 8: Address 1E.87**

### 6.11.18 Global Programmable MMD Register 9: Address 1E.88

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 4 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 4 [A:0] | Remapped MMD Address | R/W | 0x31C | Indicates the global register address to remap. |

*Table 6.11.18* **Global Programmable MMD Register 9: Address 1E.88**

### 6.11.19 Global Programmable MMD Register 10: Address 1E.89

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 4 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.19* **Global Programmable MMD Register 10: Address 1E.89**

### 6.11.20 Global Programmable MMD Register 11: Address 1E.8A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 5 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 5 [A:0] | Remapped MMD Address | R/W | 0x31D | Indicates the global register address to remap. |

*Table 6.11.20* **Global Programmable MMD Register 11: Address 1E.8A**

### 6.11.21 Global Programmable MMD Register 12: Address 1E.8B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 5 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.21* **Global Programmable MMD Register 12: Address 1E.8B**

### 6.11.22 Global Programmable MMD Register 13: Address 1E.8C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 6 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 6 [A:0] | Remapped MMD Address | R/W | 0x31E | Indicates the global register address to remap. |

*Table 6.11.22* **Global Programmable MMD Register 13: Address 1E.8C**

### 6.11.23 Global Programmable MMD Register 14: Address 1E.8D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 6 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.23* **Global Programmable MMD Register 14: Address 1E.8D**

### 6.11.24 Global Programmable MMD Register 15: Address 1E.8E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Matching Device Address 7 [F:B] | Programmable Device Address | R/W | 0x0F | Indicates the MDIO device address to match. |
| A:0 | Remapped MMD Address 7 [A:0] | Remapped MMD Address | R/W | 0x31F | Indicates the global register address to remap. |

*Table 6.11.24* **Global Programmable MMD Register 15: Address 1E.8E**

### 6.11.25 Global Programmable MMD Register 16: Address 1E.8F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Matching MMD Address 7 [F:0] | Programmable MMD Address | R/W | 0xFFFF | Indicates the MDIO MMD address to match. |

*Table 6.11.25* **Global Programmable MMD Register 16: Address 1E.8F**

### 6.11.26 Global NVR Interface 1: Address 1E.100

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | NVR Execute Operation | 1 = Starts NVR Operation | R/W SC | 0 | When set to 1, the NVR operation begins. Make sure to that the uP is stalled using the "uP Run Stall" bit to ensure that there is no NVR contention. |
| E | NVR Write Mode | 1 = Writes to NVR<br>0 = Reads from NVR | R/W | 0 | |

*Table 6.11.26* **Global NVR Interface 1: Address 1E.100**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| D | Freeze NVR CRC | 1 = Freeze NVR Mailbox CRC calculation register | R/W | 0 | To prevent an erroneous answer, this bit should *not* be set at the same time that the "NVR Execute Operation" bit is set. |
| C | Reset NVR CRC | 1 = Reset NVR Mailbox CRC calculation register | R/W SC | 0 | To prevent an erroneous answer, this bit should *not* be set at the same time that the "NVR Execute Operation" bit is set. |
| B | Reserved | Internal reserved - do not modify | | | |
| A | NVR Burst | 0 = Single read or write operation of up to 4 bytes<br>1 = Burst operation | R/W | 0 | When this bit is set, the operation is a burst operation where more than 32-bits is read from the NVR or written to the NVR. This bit should be set to 1 until the last burst in the read or write operation, when it should be set to 0.<br><br>This operates by gating the SPI clock, and *not* restarting it until new data is ready to be written, or the previous contents have been read. Each burst of data requires that the NVR Execute Operation bit is set to initiate the next phase. |
| 9 | Reserved | Internal reserved - do not modify | | | |
| 8 | NVR Busy | 1 = NVR is busy<br>0 = NVR is ready | RO | | When set to 1, the NVR is busy. A new NVR operation should *not* occur until this bit is 0. If the NVR clock is greater than 64/63 of the MDIO clock, this bit never needs to be polled when operating over the MDIO. |
| 7:0 | NVR Opcode [7:0] | NVR instruction opcode | R/W | 0x03 | |

*Table 6.11.26* **Global NVR Interface 1: Address 1E.100** (continued)

### 6.11.27 Global NVR Interface 2: Address 1E.101

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | NVR Mailbox CRC [F:0] | The running CRC-16 of everything passing through the NVR interface | RO | | The CRC-16 overall data is written or read through the NVR interface. The CRC-16 is calculated by dividing the data using this equation:<br>x^16 + x^12 + x^5 + 1 |

*Table 6.11.27* **Global NVR Interface 2: Address 1E.101**

### 6.11.28 Global NVR Interface 3: Address 1E.102

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | NVR Address MSW [17:10] | NVR address MSW bits [17:10] | R/W | 0x00 | Indicates the address of where to read and write from in the NVR. This addressed is self-incrementing and automatically increments after each read or write operation. The increment amount is based on the data length (for example, it increments by 4 if the data length is 4 bytes). |

*Table 6.11.28* **Global NVR Interface 3: Address 1E.102**

### 6.11.29 Global NVR Interface 4: Address 1E.103

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | NVR Address LSW [F:0] | NVR address LSW bits [F:0] | R/W | 0x0000 | The address of where to read and write from in the NVR. This is self-incrementing and automatically increments after each read or write operation. |

*Table 6.11.29* **Global NVR Interface 4: Address 1E.103**

### 6.11.30 Global NVR Interface 5: Address 1E.104

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | NVR Data MSW [1F:10] | NVR data MSW bits [1F:10] | R/W | 0x0000 | Data is stored and read-out from these registers in little-endian format for operations such as FLASH device ID, and also for the programming of the processor.<br><br>For instance, the 64K Atmel device code reads out as two bytes (0x651F) into the LSW register, whereas the datasheet indicates that 1F is the first byte read, followed by 65 as the second byte.<br><br>To burst read and write these 4 bytes in the correct order (where DD is written to address x), they should be stored as:<br><br>AA BB in the MSW<br>CC DD in the LSW |

*Table 6.11.30* **Global NVR Interface 5: Address 1E.104**

### 6.11.31 Global NVR Interface 6: Address 1E.105

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | NVR Data LSW [F:0] | NVR data LSW bits [F:0] | R/W | 0x0000 | Data is stored and read-out from these registers in little-endian format for operations such as FLASH device ID, and for the programming of the processor.<br><br>For instance, the 64K Atmel device code reads out as two bytes (0x651F) into the LSW register, whereas the datasheet indicates that 1F is the first byte read, followed by 65 as the second byte.<br><br>To burst read and write these 4 bytes in the correct order (where DD is written to address x), they should be stored as:<br><br>AA BB in the MSW<br>CC DD in the LSW |

*Table 6.11.31* **Global NVR Interface 6: Address 1E.105**

### 6.11.32 Global Mailbox Interface 1: Address 1E.200

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | uP Mailbox Execute Operation | 1 = Starts the mailbox Operation | R/W SC | 0 | Indicates that mailbox is loaded and ready. |
| E | uP Mailbox Write Mode | 1 = Writes<br>0 = Reads | R/W | 0 | Indicates the mailbox direction and operation. |
| D | Reserved | Internal reserved - do not modify | | | |
| C | Reset uP Mailbox CRC | 1 = Resets uP mailbox CRC calculation register | R/W SC | 0 | |
| B:9 | Reserved | Internal reserved - do not modify | | | |
| 8 | uP Mailbox Busy | 1 = uP mailbox busy<br>0 = uP mailbox ready | RO | | In general, the uP responds within a few processor cycles to any PIF slave request, much faster than the MDIO. If the busy is asserted over multiple MDIO polling cycles, then a hardware error may have occurred and a Global software reset or uP reset is required. |
| 7:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.32* **Global Mailbox Interface 1: Address 1E.200**

### 6.11.33 Global Mailbox Interface 2: Address 1E.201

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | uP Mailbox CRC [F:0] | The running CRC-16 of everything passing through the mailbox interface | RO | | |

*Table 6.11.33* **Global Mailbox Interface 2: Address 1E.201**

### 6.11.34 Global Mailbox Interface 3: Address 1E.202

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | uP Mailbox Address MSW [1F:10] | uP Mailbox MSW address | R/W | 0x0000 | Indicates the address of where to read and write from in the Microcontroller Mailbox. This is self-incrementing and automatically increments after each AQR107-AQR109 read and write operation. |

*Table 6.11.34* **Global Mailbox Interface 3: Address 1E.202**

### 6.11.35 Global Mailbox Interface 4: Address 1E.203

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | uP Mailbox Address LSW [F:2] | uP LSW Mailbox address [F:2] | R/W | 0x0000 | The address of where to read and write from in the Microcontroller Mailbox. This processor is self-incrementing and it automatically increments after each AQR107-AQR109 read and write operation. |
| 1:0 | uP Mailbox Address LSW Don't Care [1:0] | Least significant uP LSW Mailbox address bits [1:0] | RO | | These bits are always set to 0, since each memory access is on a 4-byte boundary. |

*Table 6.11.35* **Global Mailbox Interface 4: Address 1E.203**

### 6.11.36 Global Mailbox Interface 5: Address 1E.204

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | uP Mailbox Data MSW [1F:10] | uP Mailbox data MSW | R/W | 0x0000 | |

*Table 6.11.36* **Global Mailbox Interface 5: Address 1E.204**

### 6.11.37 Global Mailbox Interface 6: Address 1E.205

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | uP Mailbox Data LSW [F:0] | uP Mailbox data LSW | R/W | 0x0000 | |

*Table 6.11.37* **Global Mailbox Interface 6: Address 1E.205**

### 6.11.38 Global Mailbox Interface 7: Address 1E.206

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | uP Mailbox CRC Read Enable | 1 = Update uP mailbox CRC on read | R/W | 0 | |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.38* **Global Mailbox Interface 7: Address 1E.206**

### 6.11.39 Global Microprocessor Scratch Pad 1: Address 1E.300

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 1[F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.39* **Global Microprocessor Scratch Pad 1: Address 1E.300**

### 6.11.40 Global Microprocessor Scratch Pad 2: Address 1E.301

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 2 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.40* **Global Microprocessor Scratch Pad 2: Address 1E.301**

### 6.11.41 Global Startup Rate: Address 1E.31A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved_sp27 [B:0] | Reserved for future use | R/W | 0x000 | |
| 3:0 | Startup Rate [3:0] | 5 = 5G<br>4 = 2.5G<br>3 = 10G<br>2 = 1G<br>1 = 100M<br>0 = Low Power | R/W | 0x0 | |

*Table 6.11.41* **Global Startup Rate: Address 1E.31A**

### 6.11.42 Global System Configuration For 100M: Address 1E.31B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved_sp28 [4:0] | Reserved for future use | R/W | 0x00 | |
| A | PTP Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 9 | Security Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 8:7 | Rate Adaptation Method [1:0] | 0 = No Rate Adaptation<br>1 = USX Rate Adaptation<br>2 = Pause Rate Adaptation | R/W | 0x0 | |

*Table 6.11.42* **Global System Configuration For 100M: Address 1E.31B**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 6 | SerDes Silence Enable | 1 = Keep SerDes Silent During Transition<br>0 = Do *Not* Keep SerDes Silent During Transition | R/W | 0 | |
| 5 | Reset On Transition Enable | 0 = Do Not Reset System Interface For Every Transition<br>1 = Reset System Interface For Every Transition | R/W | 0 | |
| 4 | Training Enable | 0 = Disable System Interface Training<br>1 = Enable System Interface Training | R/W | 0 | |
| 3 | Autoneg Enable | 0 = Disables System Interface Autonegotiation<br>1 = Enables System Interface Autonegotiation | R/W | 0 | |
| 2:0 | SerDes Mode [2:0] | 0 = XFI<br>1 = XAUI<br>2 = RXAUI<br>3 = SGMII<br>4 = OCSGMII<br>5 = Low Power | R/W | 0x0 | |

*Table 6.11.42* **Global System Configuration For 100M: Address 1E.31B** (continued)

### 6.11.43 Global System Configuration For 1G: Address 1E.31C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved_sp29 [4:0] | Reserved for future use | R/W | 0x00 | |
| A | PTP Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 9 | Security Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 8:7 | Rate Adaptation Method [1:0] | 0 = No Rate Adaptation<br>1 = USX Rate Adaptation<br>2 = Pause Rate Adaptation | R/W | 0x0 | |
| 6 | SerDes Silence Enable | 1 = Keep SerDes Silent During Transition<br>0 = Do *Not* Keep SerDes Silent During Transition | R/W | 0 | |
| 5 | Reset On Transition Enable | 0 = Do *Not* Reset System Interface For Every Transition<br>1 = Reset System Interface For Every Transition | R/W | 0 | |
| 4 | Training Enable | 0 = Disables System Interface Training<br>1 = Enables System Interface Training | R/W | 0 | |

*Table 6.11.43* **Global System Configuration For 1G: Address 1E.31C**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | Autoneg Enable | 0 = Disables System Interface Autonegotiation<br>1 = Enables System Interface Autonegotiation | R/W | 0 | |
| 2:0 | SerDes Mode [2:0] | 0 = XFI<br>1 = XAUI<br>2 = RXAUI<br>3 = SGMII<br>4 = OCSGMII<br>5 = Low Power | R/W | 0x0 | |

*Table 6.11.43* **Global System Configuration For 1G: Address 1E.31C** (continued)

### 6.11.44 Global System Configuration For 2.5G: Address 1E.31D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved_sp30 [4:0] | Reserved for future use | R/W | 0x00 | |
| A | PTP Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 9 | Security Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 8:7 | Rate Adaptation Method [1:0] | 0 = No Rate Adaptation<br>1 = USX Rate Adaptation<br>2 = Pause Rate Adaptation | R/W | 0x0 | |

*Table 6.11.44* **Global System Configuration For 2.5G: Address 1E.31D**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 6 | SerDes Silence Enable | 1 = Keep SerDes Silent During Transition<br>0 = Do Not Keep SerDes Silent During Transition | R/W | 0 | |
| 5 | Reset On Transition Enable | 0 = Do *Not* Reset System Interface For Every Transition<br>1 = Reset System Interface For Every Transition | R/W | 0 | |
| 4 | Training Enable | 0 = Disables System Interface Training<br>1 = Enables System Interface Training | R/W | 0 | |
| 3 | Autoneg Enable | 0 = Disables System Interface Autonegotiation<br>1 = Enables System Interface Autonegotiation | R/W | 0 | |
| 2:0 | SerDes Mode [2:0] | 0 = XFI<br>1 = XAUI<br>2 = RXAUI<br>3 = SGMII<br>4 = OCSGMII<br>5 = Low Power | R/W | 0x0 | |

*Table 6.11.44* **Global System Configuration For 2.5G: Address 1E.31D** (continued)

### 6.11.45 Global System Configuration For 5G: Address 1E.31E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved_sp31 [4:0] | Reserved for future use | R/W | 0x00 | |
| A | PTP Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 9 | Security Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 8:7 | Rate Adaptation Method [1:0] | 0 = No Rate Adaptation<br>1 = USX Rate Adaptation<br>2 = Pause Rate Adaptation | R/W | 0x0 | |
| 6 | SerDes Silence Enable | 1 = Keep SerDes Silent During Transition<br>0 = Do *Not* Keep SerDes Silent During Transition | R/W | 0 | |
| 5 | Reset On Transition Enable | 0 = Do *Not* Reset System Interface For Every Transition<br>1 = Reset System Interface For Every Transition | R/W | 0 | |
| 4 | Training Enable | 0 = Disables System Interface Training<br>1 = Enables System Interface Training | R/W | 0 | |

*Table 6.11.45* **Global System Configuration For 5G: Address 1E.31E**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | Autoneg Enable | 0 = Disables System Interface Autonegotiation<br>1 = Enables System Interface Autonegotiation | R/W | 0 | |
| 2:0 | SerDes Mode [2:0] | 0 = XFI<br>1 = XAUI<br>2 = RXAUI<br>3 = SGMII<br>4 = OCSGMII<br>5 = Low Power | R/W | 0x0 | |

*Table 6.11.45* **Global System Configuration For 5G: Address 1E.31E** (continued)

### 6.11.46 Global System Configuration For 10G: Address 1E.31F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved_sp32 [4:0] | Reserved for future use | R/W | 0x00 | |
| A | PTP Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 9 | Security Enable | 1 = MACSec Security Enabled<br>0 = MACSec Security Disabled | R/W | 0 | |
| 8:7 | Rate Adaptation Method [1:0] | 0 = No Rate Adaptation<br>1 = USX Rate Adaptation<br>2 = Pause Rate Adaptation | R/W | 0x0 | |

*Table 6.11.46* **Global System Configuration For 10G: Address 1E.31F**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 6 | SerDes Silence Enable | 1 = Keep SerDes Silent During Transition<br>0 = Do *Not* Keep SerDes Silent During Transition | R/W | 0 | |
| 5 | Reset On Transition Enable | 0 = Do *Not* Reset System Interface For Every Transition<br>1 = Reset System Interface For Every Transition | R/W | 0 | |
| 4 | Training Enable | 0 = Disables System Interface Training<br>1 = Enables System Interface Training | R/W | 0 | |
| 3 | Autoneg Enable | 0 = Disables System Interface Autonegotiation<br>1 = Enables System Interface Autonegotiation | R/W | 0 | |
| 2:0 | SerDes Mode [2:0] | 0 = XFI<br>1 = XAUI<br>2 = RXAUI<br>3 = SGMII<br>4 = OCSGMII<br>5 = Low Power | R/W | 0x0 | |

*Table 6.11.46* **Global System Configuration For 10G: Address 1E.31F** (continued)

### 6.11.47 Global Microprocessor Scratch Pad 2 - 1: Address 1E.380

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 33 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.47* **Global Microprocessor Scratch Pad 2 - 1: Address 1E.380**

### 6.11.48 Global Microprocessor Scratch Pad 2 - 2: Address 1E.381

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 34 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.48* **Global Microprocessor Scratch Pad 2 - 2: Address 1E.381**

### 6.11.49 Global Microprocessor Scratch Pad 2 - 3: Address 1E.382

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 35 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.49* **Global Microprocessor Scratch Pad 2 - 3: Address 1E.382**

### 6.11.50 Global Microprocessor Scratch Pad 2 - 4: Address 1E.383

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 36 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.50* **Global Microprocessor Scratch Pad 2 - 4: Address 1E.383**

### 6.11.51 Global Microprocessor Scratch Pad 2 - 5: Address 1E.384

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 37 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.51* **Global Microprocessor Scratch Pad 2 - 5: Address 1E.384**

### 6.11.52 Global Microprocessor Scratch Pad 2 - 6: Address 1E.385

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 38 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.52* **Global Microprocessor Scratch Pad 2 - 6: Address 1E.385**

### 6.11.53 Global Microprocessor Scratch Pad 2 - 7: Address 1E.386

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 39 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.53* **Global Microprocessor Scratch Pad 2 - 7: Address 1E.386**

### 6.11.54 Global Microprocessor Scratch Pad 2 - 8: Address 1E.387

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 40 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.54* **Global Microprocessor Scratch Pad 2 - 8: Address 1E.387**

### 6.11.55 Global Microprocessor Scratch Pad 2 - 9: Address 1E.388

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 41 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.55* **Global Microprocessor Scratch Pad 2 - 9: Address 1E.388**

### 6.11.56 Global Microprocessor Scratch Pad 2 - 10: Address 1E.389

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 42 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.56* **Global Microprocessor Scratch Pad 2 - 10: Address 1E.389**

### 6.11.57 Global Microprocessor Scratch Pad 2 - 11: Address 1E.38A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 43 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.57* **Global Microprocessor Scratch Pad 2 - 11: Address 1E.38A**

### 6.11.58 Global Microprocessor Scratch Pad 2 - 12: Address 1E.38B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 44 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.58* **Global Microprocessor Scratch Pad 2 - 12: Address 1E.38B**

### 6.11.59 Global Microprocessor Scratch Pad 2 - 13: Address 1E.38C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 45 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.59* **Global Microprocessor Scratch Pad 2 - 13: Address 1E.38C**

### 6.11.60 Global Microprocessor Scratch Pad 2 - 14: Address 1E.38D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 46 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.60* **Global Microprocessor Scratch Pad 2 - 14: Address 1E.38D**

### 6.11.61 Global Microprocessor Scratch Pad 2 - 15: Address 1E.38E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 47 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.61* **Global Microprocessor Scratch Pad 2 - 15: Address 1E.38E**

### 6.11.62 Global Microprocessor Scratch Pad 2 - 16: Address 1E.38F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 48 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.62* **Global Microprocessor Scratch Pad 2 - 16: Address 1E.38F**

### 6.11.63 Global Microprocessor Scratch Pad 2 - 17: Address 1E.390

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 49 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.63* **Global Microprocessor Scratch Pad 2 - 17: Address 1E.390**

### 6.11.64 Global Microprocessor Scratch Pad 2 - 18: Address 1E.391

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 50 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.64* **Global Microprocessor Scratch Pad 2 - 18: Address 1E.391**

### 6.11.65 Global Microprocessor Scratch Pad 2 - 19: Address 1E.392

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 51 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.65* **Global Microprocessor Scratch Pad 2 - 19: Address 1E.392**

### 6.11.66 Global Microprocessor Scratch Pad 2 - 20: Address 1E.393

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 52 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.66* **Global Microprocessor Scratch Pad 2 - 20: Address 1E.393**

### 6.11.67 Global Microprocessor Scratch Pad 2 - 21: Address 1E.394

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 53 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.67* **Global Microprocessor Scratch Pad 2 - 21: Address 1E.394**

### 6.11.68 Global Microprocessor Scratch Pad 2 - 22: Address 1E.395

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 54 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.68* **Global Microprocessor Scratch Pad 2 - 22: Address 1E.395**

### 6.11.69 Global Microprocessor Scratch Pad 2 - 23: Address 1E.396

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 55 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.69* **Global Microprocessor Scratch Pad 2 - 23: Address 1E.396**

### 6.11.70 Global Microprocessor Scratch Pad 2 - 24: Address 1E.397

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 56 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.70* **Global Microprocessor Scratch Pad 2 - 24: Address 1E.397**

### 6.11.71 Global Microprocessor Scratch Pad 2 - 25: Address 1E.398

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 57 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.71* **Global Microprocessor Scratch Pad 2 - 25: Address 1E.398**

### 6.11.72 Global Microprocessor Scratch Pad 2 - 26: Address 1E.399

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 58 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.72* **Global Microprocessor Scratch Pad 2 - 26: Address 1E.399**

### 6.11.73 Global Microprocessor Scratch Pad 2 - 27: Address 1E.39A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 59 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.73* **Global Microprocessor Scratch Pad 2 - 27: Address 1E.39A**

### 6.11.74 Global Microprocessor Scratch Pad 2 - 28: Address 1E.39B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 60 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.74* **Global Microprocessor Scratch Pad 2 - 28: Address 1E.39B**

### 6.11.75 Global Microprocessor Scratch Pad 2 - 29: Address 1E.39C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 61 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.75* **Global Microprocessor Scratch Pad 2 - 29: Address 1E.39C**

### 6.11.76 Global Microprocessor Scratch Pad 2 - 30: Address 1E.39D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 62 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.76* **Global Microprocessor Scratch Pad 2 - 30: Address 1E.39D**

### 6.11.77 Global Microprocessor Scratch Pad 2 - 31: Address 1E.39E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 63 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.77* **Global Microprocessor Scratch Pad 2 - 31: Address 1E.39E**

### 6.11.78 Global Microprocessor Scratch Pad 2 - 32: Address 1E.39F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Scratch Pad 64 [F:0] | General Purpose Scratch Pad | R/W | 0x0000 | |

*Table 6.11.78* **Global Microprocessor Scratch Pad 2 - 32: Address 1E.39F**

### 6.11.79 Global Control 1: Address 1E.C000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.79* **Global Control 1: Address 1E.C000**

### 6.11.80 Global Control 2: Address 1E.C001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | uP Reset | 1 = Reset | R/W | 0 | Resets the uP and the PIF master and slave bus; remains active for a minimum of 100 microseconds. |
| E:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | uP Run Stall Override | 0 = uP Run Stall from “MDIO Boot Load” pin<br>1 = uP Run Stall from "uP Run Stall" bit | R/W | 0 | Bit selects the uP Run Stall from either the “MDIO Boot Load” pin or the "uP Run Stall" bit (pin no longer brought out as deprecated). |
| 5:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | uP Run Stall | 1 = uP Run Stall<br>0 = uP normal mode | R/W | 0 | Deactivates the uP. |

*Table 6.11.80* **Global Control 2: Address 1E.C001**

### 6.11.81 Global Reset Control: Address 1E.C006

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | Global MMD Reset Disable | 1 = Disables the software reset of the Global MMD registers<br>0 = Enables the software reset of the Global MMD registers | R/W PD | 0 | Setting this bit prevents a gobal software reset or global software reset from resetting the Global MMD registers. |
| D:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.81* **Global Reset Control: Address 1E.C006**

### 6.11.82 Global Diagnostic Provisioning: Address 1E.C400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Enable Diagnostics | 1 = Chip performs diagnostics upon power-up | R/W PD | 1 | |
| E:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.82* **Global Diagnostic Provisioning: Address 1E.C400**

### 6.11.83 Global Thermal Provisioning 1: Address 1E.C420

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved 0 [F:0] | Internal reserved - do not modify | R/W PD | 0x0000 | |

*Table 6.11.83* **Global Thermal Provisioning 1: Address 1E.C420**

### 6.11.84 Global Thermal Provisioning 2: Address 1E.C421

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | High Temp Failure Threshold [F:0] | [F:0] of high temperature failure threshold | R/W PD | 0x4600 | 2's complement value with the LSB representing 1/256$^{th}$ of a degree Celsius. This corresponds to -40°C = 0xD800; the default is 70°C.<br><br>**Note:** All thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds. For example, the High-Temperature-Warning (1E.C423) could be higher than the High-Temperature-Failure (1E.C421). |

*Table 6.11.84* **Global Thermal Provisioning 2: Address 1E.C421**

### 6.11.85 Global Thermal Provisioning 3: Address 1E.C422

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Low Temp Failure Threshold [F:0] | [F:0] of low temperature failure threshold | R/W PD | 0x0000 | 2's complement value with the LSB representing 1/256$^{th}$ of a degree Celsius. This corresponds to -40°C = 0xD800; the default is 0°C.<br><br>**Note:** All thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds. For example, the High-Temperature-Warning (1E.C423) could be higher than the High-Temperature-Failure (1E.C421). |

*Table 6.11.85* **Global Thermal Provisioning 3: Address 1E.C422**

### 6.11.86 Global Thermal Provisioning 4: Address 1E.C423

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | High Temp Warning Threshold [F:0] | [F:0] of high temperature warning threshold | R/W PD | 0x3C00 | 2's complement value with the LSB representing 1/256$^{th}$ of a degree Celsius. This corresponds to -40°C = 0xD008; the default is 60°C.<br><br>**Note:** All thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds. For example, the High-Temperature-Warning (1E.C423) could be higher than the High-Temperature-Failure (1E.C421). |

*Table 6.11.86* **Global Thermal Provisioning 4: Address 1E.C423**

### 6.11.87 Global Thermal Provisioning 5: Address 1E.C424

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Low Temp Warning Threshold [F:0] | [F:0] of low temperature warning threshold | R/W PD | 0x0A00 | 2's complement value with the LSB representing 1/256$^{th}$ of a degree Celsius. This corresponds to -40°C = 0xD800. Default is 10°C.<br><br>**Note:** All thresholds are orthogonal and can be set to any value regardless of the value of the other thresholds. For example, the High-Temperature-Warning (1E.C423) could be higher than the High-Temperature-Failure (1E.C421). |

*Table 6.11.87* **Global Thermal Provisioning 5: Address 1E.C424**

### 6.11.88 Enhanced LED Provisioning 1: Address 1E.C425

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:8 | LED Timer On Duration 0 [6:0] | LED On Duration 0 | R/W PD | 0x00 | The duration of turning on in the first period of LED timer (in units of 21ms). |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | LED Timer Off Duration 0 [6:0] | LED Off Duration 0 | R/W PD | 0x00 | The duration of turning off in the first period of LED timer (in units of 21ms). |

*Table 6.11.88* **Enhanced LED Provisioning 1: Address 1E.C425**

### 6.11.89 Enhanced LED Provisioning 2: Address 1E.C426

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:8 | LED Timer On Duration 1 [6:0] | LED On Duration 1 | R/W PD | 0x00 | The duration for turning on in the second period of the LED timer (in units of 21ms), (for AQRate GEN2 PHY). |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | LED Timer Off Duration 1 [6:0] | LED Off Duration 1 | R/W PD | 0x00 | The duration for turning off in the second period of the LED timer (in units of 21ms), (for AQRate GEN2 PHY). |

*Table 6.11.89* **Enhanced LED Provisioning 2: Address 1E.C426**

### 6.11.90 Enhanced LED Provisioning 3: Address 1E.C427

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Reserved | Internal reserved - do not modify | | | |
| 9:8 | LED Link Activity Mode [1:0] | 0 = No link activity<br>1 = RX link activity<br>2 = TX link activity<br>3 = Both RX and TX link activities | R/W PD | 0x0 | Selects the type of link activity for LED blinking. When it is set to 0, the timer is configured by on/off duration registers. Otherwise, timer duration is configured by the link activity LUT (for AQRate GEN2 PHY). |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:4 | LED#1 Mode [2:0] | 0 = Always off<br>1 = Always on<br>2 = Timer off (Durations 0 and 1)<br>3 = Timer on (Durations 0 and 1)<br>4 = Timer off (Duration 0)<br>5 = Timer on (Duration 0)<br>6 = Timer off (Duration 1)<br>7 = Timer on (Duration 1) | R/W PD | 0x0 | Configures when to turn on LED #1, (for AQRate GEN2 PHY). |
| 3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | LED#0 Mode [2:0] | 0 = Always off<br>1 = Always on<br>2 = Timer off (Durations 0 and 1)<br>3 = Timer on (Durations 0 and 1)<br>4 = Timer off (Duration 0)<br>5 = Timer on (Duration 0)<br>6 = Timer off (Duration 1)<br>7 = Timer on (Duration 1) | R/W PD | 0x0 | Configures when to turn on LED #0, (for AQRate GEN2 PHY). |

*Table 6.11.90* **Enhanced LED Provisioning 3: Address 1E.C427**

### 6.11.91 Enhanced LED Provisioning 4: Address 1E.C428

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 0 [5:0] | LED Link Activity LUT 0 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is equal to 0 in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 1 [5:0] | LED Link Activity LUT 1 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than 0, but smaller than 10 in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.91* **Enhanced LED Provisioning 4: Address 1E.C428**

### 6.11.92 Enhanced LED Provisioning 5: Address 1E.C429

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 2 [5:0] | LED Link Activity LUT 2 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than 10, but smaller than 100 in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 3 [5:0] | LED Link Activity LUT 3 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than 100, but smaller than 500 in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.92* **Enhanced LED Provisioning 5: Address 1E.C429**

### 6.11.93 Enhanced LED Provisioning 6: Address 1E.C42A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 4 [5:0] | LED Link Activity LUT 4 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than 500, but smaller than 1000 in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 5 [5:0] | LED Link Activity LUT 5 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than 1000, but smaller than 5000 in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.93* **Enhanced LED Provisioning 6: Address 1E.C42A**

### 6.11.94 Enhanced LED Provisioning 7: Address 1E.C42B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 6 [5:0] | LED Link Activity LUT 6 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $5x10^3$, but smaller than $1x10^4$ in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 7 [5:0] | LED Link Activity LUT 7 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $1x10^4$, but smaller than $5x10^4$ in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.94* **Enhanced LED Provisioning 7: Address 1E.C42B**

### 6.11.95 Enhanced LED Provisioning 8: Address 1E.C42C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 8 [5:0] | LED Link Activity LUT 8 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $5x10^4$, but smaller than $1x10^5$ in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 9 [5:0] | LED Link Activity LUT 9 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $1x10^5$, but smaller than $5x10^5$ in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.95* **Enhanced LED Provisioning 8: Address 1E.C42C**

### 6.11.96 Enhanced LED Provisioning 9: Address 1E.C42D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 10 [5:0] | LED Link Activity LUT 10 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $5x10^5$, but smaller than $1x10^6$ in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 11 [5:0] | LED Link Activity LUT 11 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $1x10^6$, but smaller than $5x10^6$ in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.96* **Enhanced LED Provisioning 9: Address 1E.C42D**

### 6.11.97 Enhanced LED Provisioning 10: Address 1E.C42E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 12 [5:0] | LED Link Activity LUT 12 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $5x10^6$, but smaller than $1x10^7$ in a one-second period (for AQRate GEN2 PHY). |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Link Activity LUT 13 [5:0] | LED Link Activity LUT 13 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $1x10^7$, but smaller than $5x10^7$ in a one-second period (for AQRate GEN2 PHY). |

*Table 6.11.97* **Enhanced LED Provisioning 10: Address 1E.C42E**

### 6.11.98 Enhanced LED Provisioning 11: Address 1E.C42F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D:8 | LED Link Activity LUT 14 [5:0] | LED Link Activity LUT 14 | R/W PD | 0x00 | Duration of turning on LED timer (in units of 21ms) when the packet count is greater than $5x10^7$ in a one-second period (for AQRate GEN2 PHY). |
| 7:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.98* **Enhanced LED Provisioning 11: Address 1E.C42F**

### 6.11.99 Global LED Provisioning 1: Address 1E.C430

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | LED #0 5 Gb/s Link Established | 1 = LED is on when link connects at 5 Gb/s | R/W PD | 0 | |
| E | LED #0 2.5 Gb/s Link Established | 1 = LED is on when link connects at 2.5 Gb/s | R/W PD | 0 | |
| D:9 | Reserved Provisioning C430 [4:0] | Reserved for future use | R/W PD | 0x00 | |
| 8 | LED #0 Manual Set | 1 = LED On | R/W PD | 0 | |
| 7 | LED #0 10 Gb/s Link Established | 1 = LED is on when link connects at 10 Gb/s | R/W PD | 0 | |
| 6 | LED #0 1 Gb/s Link Established | 1 = LED is on when link connects at 1 Gb/s | R/W PD | 0 | |
| 5 | LED #0 100 Mb/s Link Established | 1 = LED is on when link connects at 100 Mb/s. | R/W PD | 0 | |
| 4 | LED #0 Connecting | 1 = LED is on when attempting to connect. | R/W PD | 0 | |
| 3 | LED #0 Receive Activity | 1 = LED toggles on receive activity | R/W PD | 0 | |
| 2 | LED #0 Transmit Activity | 1 = LED toggles on transmit activity | R/W PD | 0 | |
| 1:0 | LED #0 Activity Stretch [1:0] | [1:0]<br>0x3 = stretch activity by 100ms<br>0x2 = stretch activity by 60ms<br>0x1 = stretch activity by 28ms<br>0x0 = no stretching | R/W PD | 0x3 | |

*Table 6.11.99* **Global LED Provisioning 1: Address 1E.C430**

### 6.11.100 Global LED Provisioning 2: Address 1E.C431

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | LED #1 5 Gb/s Link Established | 1 = LED is on when link connects at 5 Gb/s | R/W PD | 0 | |
| E | LED #1 2.5 Gb/s Link Established | 1 = LED is on when link connects at 2.5 Gb/s | R/W PD | 0 | |
| D:9 | Reserved Provisioning C431 [4:0] | Reserved for future use | R/W PD | 0x00 | |
| 8 | LED #1 Manual Set | 1 = LED On | R/W PD | 0 | |
| 7 | LED #1 10 Gb/s Link Established | 1 = LED is on when link connects at 10 Gb/s | R/W PD | 0 | |
| 6 | LED #1 1 Gb/s Link Established | 1 = LED is on when link connects at 1 Gb/s | R/W PD | 0 | |
| 5 | LED #1 100 Mb/s Link Established | 1 = LED is on when link connects at 100 Mb/s. | R/W PD | 0 | |
| 4 | LED #1 Connecting | 1 = LED is on when attempting to connect. | R/W PD | 0 | |
| 3 | LED #1 Receive Activity | 1 = LED toggles on receive activity | R/W PD | 0 | |
| 2 | LED #1 Transmit Activity | 1 = LED toggles on transmit activity | R/W PD | 0 | |
| 1:0 | LED #1 Activity Stretch [1:0] | [1:0]<br>0x3 = stretch activity by 100ms<br>0x2 = stretch activity by 60ms<br>0x1 = stretch activity by 28ms<br>0x0 = no stretching | R/W PD | 0x3 | |

*Table 6.11.100* **Global LED Provisioning 2: Address 1E.C431**

### 6.11.101 Global LED Provisioning 3: Address 1E.C432

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | LED #2 5 Gb/s Link Established | 1 = LED is on when link connects at 5 Gb/s | R/W PD | 0 | |
| E | LED #2 2.5 Gb/s Link Established | 1 = LED is on when link connects at 2.5 Gb/s | R/W PD | 0 | |
| D:9 | Reserved Provisioning C432 [4:0] | Reserved for future use | R/W PD | 0x00 | |
| 8 | LED #2 Manual Set | 1 = LED On | R/W PD | 0 | |
| 7 | LED #2 10 Gb/s Link Established | 1 = LED is on when link connects at 10 Gb/s | R/W PD | 0 | |
| 6 | LED #2 1 Gb/s Link Established | 1 = LED is on when link connects at 1 Gb/s | R/W PD | 0 | |
| 5 | LED #2 100 Mb/s Link Established | 1 = LED is on when link connects at 100 Mb/s. | R/W PD | 0 | |
| 4 | LED #2 Connecting | 1 = LED is on when attempting to connect. | R/W PD | 0 | |
| 3 | LED #2 Receive Activity | 1 = LED toggles on receive activity | R/W PD | 0 | |
| 2 | LED #2 Transmit Activity | 1 = LED toggles on transmit activity | R/W PD | 0 | |
| 1:0 | LED #2 Activity Stretch [1:0] | [1:0]<br>0x3 = stretch activity by 100ms<br>0x2 = stretch activity by 60ms<br>0x1 = stretch activity by 28ms<br>0x0 = no stretching | R/W PD | 0x3 | |

*Table 6.11.101* **Global LED Provisioning 3: Address 1E.C432**

### 6.11.102 Global LED Provisioning 4: Address 1E.C433

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.102* **Global LED Provisioning 4: Address 1E.C433**

### 6.11.103 Global LED Provisioning 5: Address 1E.C434

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.103* **Global LED Provisioning 5: Address 1E.C434**

### 6.11.104 Global LED Provisioning 6: Address 1E.C435

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.104* **Global LED Provisioning 6: Address 1E.C435**

### 6.11.105 Global LED Provisioning 7: Address 1E.C436

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.105* **Global LED Provisioning 7: Address 1E.C436**

### 6.11.106 Global LED Provisioning 8: Address 1E.C437

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | LED Operation Mode 1 | 1 = LED link activity in Mode #2<br>0 = LED link activity based on "LED Operation Mode 0" setting | R/W PD | 0 | When both bit 1 and bit 0 are set to 1, the LED blinking rate is based on Mode #2 algorithm. When bit 1 is set to 0, the LED blinking rate is based on the "LED Operation Mode 0" setting (for AQRate GEN2 PHY). |
| 0 | LED Operation Mode 0 | 1 = LED link activity in Mode #2<br>0 = LED link activity in Aquantia classic mode | R/W PD | 0 | When bit 1 is set to 0 and bit 0 is set to 1, the LED blinking rate is based on Mode #2 algorithm. When both bits are set to 0, the LED blinking rate is based on the classic Aquantia algorithm.<br><br>**Note:** This bit is *only* valid when "LED Operation Mode 1" is set to 0. |

*Table 6.11.106* **Global LED Provisioning 8: Address 1E.C437**

### 6.11.107 Global LED Provisioning 15: Address 1E.C43E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.107* **Global LED Provisioning 15: Address 1E.C43E**

### 6.11.108 Global General Provisioning 1: Address 1E.C440

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.108* **Global General Provisioning 1: Address 1E.C440**

### 6.11.109 Global General Provisioning 2: Address 1E.C441

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | MDIO Broadcast Mode Enable | 1 = Enables broadcast on address set in 1E.C446<br>0 = Disables broadcast on address set in 1E.C446 | R/W PD | 0 | When enabled, writes and loading of MMD address opcodes are supported; read opcodes are ignored. |
| D | MDIO Read MSW First Enable | 1 = MSW of counter must be read first<br>0 = LSW of counter must be read first | R/W PD | 0 | Bit configures whether the MSW or LSW must be read first for counters greater than 16 bits. |
| C:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | MDIO Drive Configuration | 0 = MDIO driver is in normal mode<br>1 = MDIO driver is in open drain mode | R/W PD | 0 | When MDIO driver is in open drain mode during a read cycle, “0” data is actively driven out of MDIO, “1” data sets MDIO driver in a high impedance state and an external pull-up sets MDIO line to “1”. Turn-Around “0” is also actively driven out of MDIO; therefore, in open drain mode, Turn-Around is still “Z0”. |
| 3 | MDIO Preamble Detection Disable | 1 = Suppress preamble detection on MDIO<br>0 = Enable preamble detection on MDIO | R/W PD | 0 | |

*Table 6.11.109* **Global General Provisioning 2: Address 1E.C441**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.109* **Global General Provisioning 2: Address 1E.C441**

### 6.11.110 Global General Provisioning 3: Address 1E.C442

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Daisy Chain Reset | 1 = Resets the Daisy Chain | R/W | 0 | Toggling this bit from 0 to 1 reloads the IRAM and DRAM and resets the uP. uP is in uP run stall during the reload process. After the reload process, uP run stall is de-asserted and uP reset is asserted. Note that before setting this bit, "Soft Reset" bit needs to be de-asserted. |

*Table 6.11.110* **Global General Provisioning 3: Address 1E.C442**

### 6.11.111 Global General Provisioning 4: Address 1E.C443

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.111* **Global General Provisioning 4: Address 1E.C443**

### 6.11.112 Global General Provisioning 5: Address 1E.C444

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.112* **Global General Provisioning 5: Address 1E.C444**

### 6.11.113 Global General Provisioning 6: Address 1E.C445

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.113* **Global General Provisioning 6: Address 1E.C445**

### 6.11.114 Global General Provisioning 7: Address 1E.C446

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.114* **Global General Provisioning 7: Address 1E.C446**

### 6.11.115 Global General Provisioning 8: Address 1E.C447

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4:0 | MDIO Broadcast Address Configuration [4:0] | Broadcast address | R/W PD | 0x00 | Allows for setting the broadcast address (by default, this is set to 0x00). |

*Table 6.11.115* **Global General Provisioning 8: Address 1E.C447**

### 6.11.116 Global General Provisioning 9: Address 1E.C448

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.116* **Global General Provisioning 9: Address 1E.C448**

### 6.11.117 Global General Provisioning 10: Address 1E.C449

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6:0 | MDIO Preamble Length [6:0] | MDIO Preamble Length | R/W | 0x02 | |

*Table 6.11.117* **Global General Provisioning 10: Address 1E.C449**

### 6.11.118 Global NVR Provisioning 1: Address 1E.C450

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved | Internal reserved - do not modify | | | |
| A:8 | NVR Data Length [2:0] | NVR data length ranges from 0 bytes to 4 bytes | R/W PD | 0x4 | Sets the length of the data burst used in read and write operations. |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:4 | NVR Dummy Length [2:0] | NVR dummy length ranges from 0 bytes to 4 bytes | R/W PD | 0x0 | Sets the length of the dummy field used in some manufacturer's read status and write status operations. |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | NVR Address Length [1:0] | NVR address length ranges from 0 bytes up to 3 bytes | R/W PD | 0x2 | Sets the length of the address field used in read and write operations. Use of this field is enabled via Bit 8 of "Global NVR Provisioning 2: Address 1E.C451" on page 530. |

*Table 6.11.118* **Global NVR Provisioning 1: Address 1E.C450**

### 6.11.119 Global NVR Provisioning 2: Address 1E.C451

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:9 | Reserved | Internal reserved - do not modify | | | |
| 8 | NVR Address Length Override | 0 = NVR address length is based on the "NVR_SIZE" pin.<br>1 = NVR address length is based on the "NVR Address Length [1:0]" register | R/W PD | 0 | When this bit = 0 and NVR_SIZE pin = 0, the NVR address length is 2 bytes.<br><br>When this bit = 0 and the NVR_SIZE pin = 1, the NVR address length is 3 bytes.<br><br>When this bit = 1, the NVR address length is determined by: "NVR Address Length [1:0]" value. |
| 7:0 | NVR Clock Divide [7:0] | NVR clock divide; clock frequency is divided by the NVR clock divide + 1 | R/W PD | 0xA0 | |

*Table 6.11.119* **Global NVR Provisioning 2: Address 1E.C451**

### 6.11.120 Global NVR Provisioning 3: Address 1E.C452

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:2 | Reserved | Internal reserved - do not modify | | | |
| 1 | NVR Daisy Chain Clock Divide Override | 1 = Overrides NVR clock divide when in Daisy Chain master mode | R/W | 0 | When in Daisy Chain master mode, the clock divide configuration is received from the FLASH, and this bit overrides the clock divide configuration from the FLASH with the "NVR Clock Divide [7:0]" value. |
| 0 | NVR Daisy Chain Disable | 1 = Disables the Daisy Chain | R/W | 0 | When in Daisy Chain master mode, the Daisy Chain and MDIO can both access the SPI. Setting this bit to 1 disables the Daisy Chain from accessing the SPI and force it into a reset state. |

*Table 6.11.120* **Global NVR Provisioning 3: Address 1E.C452**

### 6.11.121 Global NVR Provisioning 4: Address 1E.C453

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | NVR Reset | 1 = Resets SPI | R/W | 0 | |
| 3:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.121* **Global NVR Provisioning 4: Address 1E.C453**

### 6.11.122 Global Reserved Provisioning 1: Address 1E.C470

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Diagnostics Select | 1 = Provides Extended MDI Diagnostics Information.<br>0 = Provides normal cable diagnostics | R/W PD | 0 | Bits select what sort of cable diagnostics to perform. For regular cable diagnostics, Bit F is set to zero, and the diagnostics are triggered by setting Bit 4. For extended diagnostics, Bit F is set to 1, and the desired extended diagnostics are selected by Bits E:D and routine is triggered by setting Bit 4. Each of the extended diagnostic routines present data for all for MDI pairs (A, B, C, D) consecutively, and after the data for each channel is gathered Bits F:D are reset. To get the data for the next pair, Bits F:D must be set back to the desired value (which must be the same as the initial channel). This process continues until the data for all channels has been gathered. The address in memory where the data is stored is given in 1E.C802 and 1E.C804.<br><br>For the case of PSD, the structure is as follows:<br>Int32 info<br>Int16 data[Len]<br>Info = Len << 16 \| TX Enable << 8 \| Pair (0 = A, etc.)<br><br>For TDR:<br>Int32 info<br>Int16 tdr_A[Len]<br>Int16 tdr_B[Len]<br>Int16 tdr_C[Len]<br>Int16 tdr_D[Len]<br><br>Info = Len << 16 \| Channel<br><br>TDR data is from the current pair to all other pairs.<br><br>At the end of retrieving extended MDI diag data, the part is reset. Conversely, the only way to exit this routine once it starts is to issue a PMA reset. |
| E:D | Extended MDI Diagnostics Select [1:0] | 0x0 = TDR Data<br>0x1 = RFI Channel PSD<br>0x2 = Noise PSD while the local TX is Off<br>0x3 = Noise PSD while the local TX is On | R/W PD | 0x0 | |

*Table 6.11.122* **Global Reserved Provisioning 1: Address 1E.C470**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| C:8 | Reserved | Internal reserved - do not modify | | | |
| 7 | Trigger Diagnostic Interrupt | 1 = Triggers Diagnostic Interrupt | R/W SC | 0 | |
| 6:5 | Reserved | Internal reserved - do not modify | | | |
| 4 | Initiate Cable Diagnostics | 1 = Performs cable diagnostics | R/W SC | 0 | Performs cable diagnostics regardless of link state. If link is up, setting this bit causes the link to drop while diagnostics are performed. This bit is self-clearing upon completion of the cable diagnostics.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can also be monitored via 1E.C831.F. |
| 3:2 | Reserved | Internal reserved - do not modify | | | |
| 1:0 | Cable Diagnostics Baud Rates | 0b00 = 0<br>Sets 800M baud rate for measuring faults and cable lengths up to 100 meters with the highest resolution<br><br>0b01 = 1<br>Sets 400M baud rate for measuring faults and cables lengths up to 200 meters (with half the resolution of the 800M baud cable diagnostics)<br><br>0b10 = 2<br>Reserved<br><br>0b11 = 3<br>Reserved | R/W SC | 0 | **Note:** These settings select the baud rate at which the cable diagnostics are run by the firmware:<br><br>-- 800M baud covers the 400MHz bandwidth with the highest resolution.<br><br>-- 400M baud covers the 200MHz bandwidth with half the resolution of 800M baud. |

*Table 6.11.122* **Global Reserved Provisioning 1: Address 1E.C470** (continued)

### 6.11.123 Global Reserved Provisioning 2: Address 1E.C471

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Enable Daisy Chain Hop-Count Override | 1 = Hop-count is set by Bits 5:0<br>0 = Hop-count is determined by the Daisy Chain | R/W uP | 0 | Daisy Chain Hop-Count Override should be used during MDIO boot-load operation, as the Daisy Chain hop-count does not function when Daisy Chain is disabled (1E.C452.0).<br><br>Setting this bit tells the processor where in the Daisy Chain it is, so that provisioning operation will function correctly. |
| 5:0 | Daisy Chain Hop-Count Override Value [5:0] | Uses this value for PHY Daisy Chain hop-count; valid values are from 0 to 47 | R/W uP | 0x00 | |

*Table 6.11.123* **Global Reserved Provisioning 2: Address 1E.C471**

### 6.11.124 Global Reserved Provisioning 3: Address 1E.C472

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | Enable VDD Power Supply Tuning | 1 = Enables external VDD power supply tuning<br>0 = Disables external VDD power supply tuning is disabled | R/W PD | 0 | Bit controls whether the PHY attempts to tune the external VDD power supply via the SMBus. Note that this bit is only operational if the external supply is present (see 1E.C472.6). |
| D:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Tunable External VDD Power Supply Present | 1 = Tunable external VDD power supply present<br>0 = No tunable external VDD power supply present | R/W PD | 0 | Bit must be set if tuning of external power supply is desired. |

*Table 6.11.124* **Global Reserved Provisioning 3: Address 1E.C472**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5:2 | External VDD Change Request [3:0] | The amount of VDD change requested by firmware, in mV (2's complement value) | R/W PD | 0x0 | |
| 1 | Enable Register Space | 1 = Register space enabled<br>0 = Register space disabled | R/W PD uP | 0 | |
| 0 | Enable 5th Channel RFI Cancellation | 1 = 5th channel and RFI cancellers operation enabled<br>0 = 5th channel AFE is powered down, 5th channel digital is clock gated, RFI cancellers are disabled | R/WP D uP | 0 | **Note:** Represents the value of this bit at the time of autonegotiation, which sets the local PHY behavior until the next time that autonegotiation occurs. |

*Table 6.11.124* **Global Reserved Provisioning 3: Address 1E.C472**

### 6.11.125 Global Reserved Provisioning 4: Address 1E.C473

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.125* **Global Reserved Provisioning 4: Address 1E.C473**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A:8 | Rate Transition Request [2:0] | 0 = No Transition<br>1 = Reserved<br>2 = Reserved<br>3 = Retrain at 10G<br>4 = Retrain at 5G<br>5 = Retrain at 2.5G<br>6 = Retrain at 1G<br>7 = Reserved | R/W PD | 0x0 | |
| 7:0 | Training SNR [7:0] | SNR during 10G training on the worst channel. SNR is in steps of 0.1dB | R/W PD | 0x00 | The SNR margin that is enjoyed by the worst channel, over and above the minimum SNR required to operate at a BER of $10^{-12}$. It is reported with 0.1dB of resolution to an accuracy of 0.5dB within the range of -12.7dB to 12.7dB. The number is in offset binary, with 0.0dB represented by 0x8000. |

*Table 6.11.125* **Global Reserved Provisioning 4: Address 1E.C473**

### 6.11.126 Global Reserved Provisioning 5: Address 1E.C474

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved Provisioning 5 [F:1] | Reserved for future use | R/W PD | 0x0000 | |
| 0 | NVR Daisy Chain Kickstart | 1 = Kickstart the Daisy Chain | R/W | 0 | When in Daisy Chain master mode, the PHY0 can kickstart the Daisy Chain. The kickstart will *not* reload the IRAM/DRAM or reset the uP for PHY0; it will read the FLASH and transfer the FLASH data to the Daisy Chain. |

*Table 6.11.126* **Global Reserved Provisioning 5: Address 1E.C474**

### 6.11.127 Global Reserved Provisioning 6: Address 1E.C475

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Internal reserved - do not modify | | | |
| D | Smart Power-Down Status | 1 = Smart Power-Down Active<br>0 = Smart Power-Down Inactive | R/W PD | 0 | |
| C | Reserved Provisioning 6 | Internal reserved - do not modify | R/W PD | 0 | |
| B | CFR LP Disable Timer | 1 = Link partner requires cfr_disable timer<br>0 = Link partner does *not* require cfr_disable timer | R/W PD | 0 | |
| A | CFR LP Extended Maxwait | 1 = Link partner requires extended maxwait<br>0 = Link partner does *not* require extended maxwait | R/W PD | 0 | |
| 9 | CFR LP THP | 1 = Link partner requires local PHY to enable THP<br>0 = Link partner does *not* require local PHY to enable THP | R/W PD | 0 | |
| 8 | CFR LP Support | 1 = Link partner supports Cisco Fast Retrain (CFR)<br>0 = Link partner does support Cisco Fast Retrain | R/W PD | 0 | |

*Table 6.11.127* **Global Reserved Provisioning 6: Address 1E.C475**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | CFR Disable Timer | 1 = Local PHY requires cfr_disable timer<br>0 = Local PHY does *not* require cfr_disable timer | R/W PD | 0 | |
| 6 | CFR Extended Maxwait | 1 = Local PHY requires extended maxwait<br>0 = Local PHY does *not* require extended maxwait | R/W PD | 0 | |
| 5 | CFR THP | 1 = Local PHY requires local PHY to enable THP<br>0 = Local PHY does *not* require local PHY to enable THP | R/W PD | 0 | |
| 4 | CFR Support | 1 = Local PHY supports Cisco Fast Retrain<br>0 = Local PHY does support Cisco Fast Retrain | R/W PD | 0 | |
| 3 | Deadlock Avoidance Enable | 1 = SPD with deadlock avoidance: PHY transmits autonegotiation pulses (FLPs) at a slower rate (~ 1 FLP/100ms) than specified by autonegotiation standard (~1 FLP/8.25ms); receiver is active and able to detect the pulses<br>0 = SPD without deadlock avoidance: PHY transmitter is shut down, no autonegotiation pulses are sent on the line, but the receiver is active and able to detect the pulses | R/W PD | 0 | |

*Table 6.11.127* **Global Reserved Provisioning 6: Address 1E.C475** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Smart Power Down Enable | 1 = Enables Smart Power Down mode<br>0 = Disables Smart Power Down mode | R/W PD | 0 | Smart Power Down (SPD) is the lowest power mode at which PHY is able to autonegotiate. SPD can be enabled with bit 1E.C475.2. |
| 1:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.127* **Global Reserved Provisioning 6: Address 1E.C475** (continued)

### 6.11.128 Global Reserved Provisioning 9: Address 1E.C478

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | DTE Enable | 1 = Enables DTE<br>0 = Disables DTE | R/W PD | 0 | |
| E:B | DTE Drop Reporting Timer [3:0] | Number of seconds between loss of the link partner filter and assertion of a no-power-needed state, in 5 second increments (for example, 0x4 = 20 seconds) | R/W PD | 0x0 | Bits are used to set how long the PHY waits after it no longer detects the link partner filter before declaring that power is unneeded. |
| A | Thermal Shutdown Enable | 1 = PHY goes to low power mode if the current temperature exceeds the temperature threshold that was selected through this register (1E.C475.F:E) | R/W PD | 0 | Global fault is generated (1E.C850 = 0x8007) upon triggering thermal shutdown event. |

*Table 6.11.128* **Global Reserved Provisioning 9: Address 1E.C478**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 9 | SFP-DDMI Enable | 1 = PHY supports the SFP Digital Diagnostic Monitoring Interface via the SMB0 SMBus controller, at slave addresses A0 and A2 | R/W PD | 0 | Must be set via provisioning, using the POWER_UP_INIT block. |
| 8:0 | Reserved Provisioning 9 [8:0] | Reserved for future use | R/W PD | 0x000 | |

*Table 6.11.128* **Global Reserved Provisioning 9: Address 1E.C478**

### 6.11.129 Global Reserved Provisioning 10: Address 1E.C479

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Power-Up Stall | 1 = Stalls firmware at Power-Up<br>0 = Prevents stall of the firmware | R/W PD | 0 | Bit needs to be provisioned in Power-Up Init for the firmware to stall. |

*Table 6.11.129* **Global Reserved Provisioning 10: Address 1E.C479**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| E:4 | Reserved Provisioning 10 [A:0] | Reserved for future use | R/W PD | 0x000 | |
| 3:0 | Enhanced LED Modes | 0 - 0x9 = Reserved<br>0xA = LEDs are set based on link status and activity determined by PHY from autonegotiation registers<br>0xB = LEDs are set based on system software determining CR and runt errors<br>0xC = LEDs are set based on system software determining status of STP port<br>0xD = LEDs are set based on software determining the status of STP port, but receiving/sending data<br>0xE = LEDs are set by PHY based on speed and timer programming<br>0xF = Reserved | R/W PD | 0x0 | |

*Table 6.11.129* **Global Reserved Provisioning 10: Address 1E.C479**

### 6.11.130 Global Reserved Provisioning 11: Address 1E.C47A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Loopback Control [4:0] | 0x00 = No loopback<br>0x01 = System Interface - System Loopback<br>0x02 = System Interface - System Loopback with Passthrough<br>0x03 = System Interface - Network Loopback<br>0x04 = System Interface - Network Loopback with Passthrough<br>0x05 = System Interface - Network Loopback with Passthrough and Merge<br>0x06 = System Interface - Peer-to-peer loopback<br>0x07 - 0x08 = Reserved<br>0x09 = Network Interface - System Loopback<br>0x0A = Network Interface - System Loopback with Passthrough<br>0x0B = Network Interface - Network Loopback<br>0x0C = Network Interface - Network Loopback with Passthrough<br>0x0D = Network Interface - Peer-to-peer loopback<br>0x0E - 0x0F = Reserved<br>0x10 = Cross-connect System Loopback<br>0x11 = Cross-connect Network Loopback<br>0x12 - 0x13 = Reserved<br>0x14 = Network Interface - System Loopback via Loopback Plug<br>0x15 - 0x1F = Reserved | R/W PD | 0x00 | These bits, in conjunction with the chip configuration and the rate (Bits 1:0), select the loopback for configuring the chip.<br><br>Setting one of these loopbacks provisions the chip for the specified loopback. Upon clearing the loopback, the chip returns to its prior configuration before it entered loopback (regardless of whether other loopbacks were selected after the initial loopback).<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F.<br><br>Note that the controls in this register are identical to, and mirrored with, the controls in 4.C444. |
| A:6 | Reserved Provisioning 11 [4:0] | Reserved for future use | R/W PD | 0x00 | |

*Table 6.11.130* **Global Reserved Provisioning 11: Address 1E.C47A**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | MDI Packet Generation | 1 = CRPAT packet generation out MDI interface<br>0 = No CRPAT packet generation out MDI interface | R/W PD | 0 | Selecting this mode causes the CRPAT packet generator in the PHY to output on the MDI interface at the selected rate.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F.<br><br>Note that the controls in this register are identical to, and mirrored with, the controls in 4.C444. |
| 4 | Look-Aside Port Packet Generation | 1 = CRPAT packet generation out 10G look-aside interface (KR0)<br>0 = No CRPAT packet generation out 10G look-aside interface (KR0) | R/W PD | 0 | Selecting this mode causes the CRPAT packet generator in the PHY to output on KR0.<br><br>**Note:** This only functions if KR1 (SERDES2) is selected as the system interface in (4.C441.F:E).<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F.<br><br>Note that the controls in this register are identical to, and mirrored with, the controls in 4.C444. |

*Table 6.11.130* **Global Reserved Provisioning 11: Address 1E.C47A** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | System I/F Packet Generation | 1 = CRPAT packet generation out 10G system interface<br>0 = No CRPAT packet generation out 10G system interface | R/W PD | 0 | Selecting this mode causes the CRPAT packet generator in the PHY to output CRPAT packets on the selected 10G system interface (4.C441.F:E)<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F.<br><br>Note that the controls in this register are identical to, and mirrored with, the controls in 4.C444. |
| 2:0 | Rate [2:0] | 0x7 - 0x6 = Reserved<br>0x5 = 5G<br>0x4 = 2.5G<br>0x3 = 10G<br>0x2 = 1G<br>0x1 = 100M<br>0x0 = Reserved | R/W PD | 0x0 | These bits select the rate for the loopback and packet generation. SerDes configuration, as well autonegotiation, is controlled accordingly when a loopback is selected.<br><br>For instance, if 100M system loopback on the network interface is selected, SGMII on the system interface is enabled to connect at 100M, and if passthrough is enabled, then 100BASE-TX is the only advertised rate and forces a re-autonegotiation if *not* already connected at 100M.<br><br>**Note:** This is a processor-intensive operation. Completion of this operation can be monitored via 1E.C831.F.<br><br>Note that the controls in this register are identical to, and mirrored with, the controls in 4.C444. |

*Table 6.11.130* **Global Reserved Provisioning 11: Address 1E.C47A** (continued)

### 6.11.131 Global Reserved Provisioning 12: Address 1E.C47B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Provisioning 12 [F:0] | Reserved for future use | R/W PD | 0x0000 | |

*Table 6.11.131* **Global Reserved Provisioning 12: Address 1E.C47B**

### 6.11.132 PIF Mailbox Control 1: Address 1E.C47C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PIF Mailbox Address [F:0] | Address (lower 16 bits) specifying the target register to read or write | R/W PD uP | 0x0000 | Specifies the first target register. |

*Table 6.11.132* **PIF Mailbox Control 1: Address 1E.C47C**

### 6.11.133 PIF Mailbox Control 2: Address 1E.C47D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | PIF Mailbox Data [F:0] | Data to be written, or that has been read from, the target register | R/W PD uP | 0x0000 | |

*Table 6.11.133* **PIF Mailbox Control 2: Address 1E.C47D**

### 6.11.134 PIF Mailbox Control 3: Address 1E.C47E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:D | Reserved PIF Mailbox Control 3 [2:0] | Reserved for future use | R/W PD | 0x0 | |
| C | Service Second Register | 0 = Handles the read/write request for only the first target register<br>1 = Handles the read/write request for both the first and second target registers | R/W PD uP | 0 | Either one or two target registers can be read from or written to:<br><br>If set to 1, then the first target register is read/ from/written to, then the second target register is read from /written to. The second target register is specified by the PIF Mailbox Extra group (4.E41D - 4.E41F).<br><br>If this bit is 0, *only* the first target register is read from/written to, and the PIF Mailbox Extra registers are ignored. |
| B:8 | PIF Mailbox Command Type [3:0] | 0 = No Action<br>1 = Reads<br>2 = Writes | R/W PD uP | 0x0 | The PIF Mailbox supports reading/writing arbitrary (“target”) PHY registers indirectly, via the uP’s PIF interface. This is an alternative register accessing mechanism to MDIO or SMBus.<br><br>System software writes non-zero value to start a PIF command. |
| 7:0 | PIF Mailbox MMD [7:0] | MMD (upper 8 bits) specifying the target register to read or write. | R/W PD uP | 0x00 | Specifies the first target register. |

*Table 6.11.134* **PIF Mailbox Control 3: Address 1E.C47E**

### 6.11.135 PIF Mailbox Control 4: Address 1E.C47F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:4 | Reserved PIF Mailbox Control 4 [B:0] | Reserved for future use | R/W PD | 0x000 | |
| 3:0 | PIF Mailbox Command Status [3:0] | 0 = Idle<br>1 = Command completed<br>2 = Command did *not* complete | R/W PD uP | 0x0 | System software should write 0 before writing Command Type to clear completion status. |

*Table 6.11.135* **PIF Mailbox Control 4: Address 1E.C47F**

### 6.11.136 Global SMBus 0 Provisioning 6: Address 1E.C485

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:1 | SMB 0 Slave Address [7:1] | SMB slave address configuration | R/W | 0x00 | |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.136* **Global SMBus 0 Provisioning 6: Address 1E.C485**

### 6.11.137 Global SMBus 1 Provisioning 6: Address 1E.C495

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:1 | SMB 1 Slave Address [7:1] | SMB slave address configuration | R/W | 0x00 | |
| 0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.137* **Global SMBus 1 Provisioning 6: Address 1E.C495**

### 6.11.138 Global EEE Provisioning 1: Address 1E.C4A0

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | EEE Mode | 1 = EEE mode of operation | R/W PD | 0 | Indicates the EEE mode of operation (0 = disabled, 1 = enabled; default: 0). |

*Table 6.11.138* **Global EEE Provisioning 1: Address 1E.C4A0**

### 6.11.139 Global Cable Diagnostic Status 1: Address 1E.C800

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E:C | Pair A Status [2:0] | [F:D]<br>111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>011 = Connected to Pair D<br>010 = Connected to Pair C<br>001 = Connected to Pair B<br>000 = OK | RO | | This register summarizes the worst impairment on Pair A. |
| B | Reserved | Internal reserved - do not modify | | | |
| A:8 | Pair B Status [2:0] | [C:A]<br>111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>011 = Connected to Pair A<br>010 = Connected to Pair D<br>001 = Connected to Pair C<br>000 = OK | RO | | This register summarizes the worst impairment on Pair B. |
| 7 | Reserved | Internal reserved - do not modify | | | |
| 6:4 | Pair C Status [2:0] | [9:7]<br>111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>011 = Connected to Pair B<br>010 = Connected to Pair A<br>001 = Connected to Pair D<br>000 = OK | RO | | This register summarizes the worst impairment on Pair C. |

*Table 6.11.139* **Global Cable Diagnostic Status 1: Address 1E.C800**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 3 | Reserved | Internal reserved - do not modify | | | |
| 2:0 | Pair D Status [2:0] | [6:4]<br>111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>011= Connected to Pair C<br>010= Connected to Pair B<br>001= Connected to Pair A<br>000= OK | RO | | This register summarizes the worst impairment on Pair D. |

*Table 6.11.139* **Global Cable Diagnostic Status 1: Address 1E.C800** (continued)

### 6.11.140 Global Cable Diagnostic Status 2: Address 1E.C801

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Pair A Reflection #1 [7:0] | Distance in meters, accurate to ±1m, of the first of the four worst reflections seen by the PHY on Pair A | RO | | The distance to this reflection is given in "Global Cable Diagnostic Impedance 1: Address 1E.C880" . A value of zero indicates that this reflection does *not* exist or was *not* computed. |
| 7:0 | Pair A Reflection #2 [7:0] | Distance in meters, accurate to ±1m, of the second of the four worst reflections seen by the PHY on Pair A | RO | | |

*Table 6.11.140* **Global Cable Diagnostic Status 2: Address 1E.C801**

### 6.11.141 Global Cable Diagnostic Status 3: Address 1E.C802

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Impulse Response MSW [F:0] | MSW of the memory location that contains the start of the impulse response data for the Extended Diagnostic type in 1E.C470.E:D | RO | | See 1E.C470 for more information. |

*Table 6.11.141* **Global Cable Diagnostic Status 3: Address 1E.C802**

### 6.11.142 Global Cable Diagnostic Status 4: Address 1E.C803

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Pair B Reflection #1 [7:0] | Distance in meters, accurate to ±1m, of the first of the four worst reflections seen by the PHY on Pair B | RO | | The distance to this reflection is given in: "Global Cable Diagnostic Impedance 2: Address 1E.C881"<br><br>A value of zero indicates that this reflection does *not* exist or was *not* computed. |
| 7:0 | Pair B Reflection #2 [7:0] | Distance in meters, accurate to ±1m, of the second of the four worst reflections seen by the PHY on Pair B | RO | | |

*Table 6.11.142* **Global Cable Diagnostic Status 4: Address 1E.C803**

### 6.11.143 Global Cable Diagnostic Status 5: Address 1E.C804

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Impulse Response LSW [F:0] | LSW of the memory location that contains the start of the impulse response data for the Extended Diagnostic type specified in 1E.C470.E:D | RO | | See 1E.C470 for more information. |

*Table 6.11.143* **Global Cable Diagnostic Status 5: Address 1E.C804**

### 6.11.144 Global Cable Diagnostic Status 6: Address 1E.C805

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Pair C Reflection #1 [7:0] | Distance in meters, accurate to ±1m, of the first of the four worst reflections seen by the PHY on Pair C | RO | | The distance to this reflection is given in: "Global Cable Diagnostic Impedance 3: Address 1E.C882"<br><br>A value of zero indicates that this reflection does *not* exist or was *not* computed. |
| 7:0 | Pair C Reflection #2 [7:0] | Distance in meters, accurate to ±1m, of the second of the four worst reflections seen by the PHY on Pair C | RO | | |

*Table 6.11.144* **Global Cable Diagnostic Status 6: Address 1E.C805**

### 6.11.145 Global Cable Diagnostic Status 7: Address 1E.C806

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved 1 [F:0] | Reserved for future use | RO | | |

*Table 6.11.145* **Global Cable Diagnostic Status 7: Address 1E.C806**

### 6.11.146 Global Cable Diagnostic Status 8: Address 1E.C807

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Pair D Reflection #1 [7:0] | Distance in meters, accurate to ±1m, of the first of the four worst reflections seen by the PHY on Pair D | RO | | The distance to this reflection is given in: "Global Cable Diagnostic Impedance 4: Address 1E.C883"<br><br>A value of zero indicates that this reflection does *not* exist or was *not* computed. |
| 7:0 | Pair D Reflection #2 [7:0] | Distance in meters, accurate to ±1m, of the second of the four worst reflections seen by the PHY on Pair D | RO | | |

*Table 6.11.146* **Global Cable Diagnostic Status 8: Address 1E.C807**

### 6.11.147 Global Thermal Status 1: Address 1E.C820

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Temperature [F:0] | [F:0] of temperature | RO | | 2's complement value with the LSB representing 1/256$^{th}$ of a degree Celsius. This corresponds to -40°C = 0xD800; default is 70°C. |

*Table 6.11.147* **Global Thermal Status 1: Address 1E.C820**

### 6.11.148 Global Thermal Status 2: Address 1E.C821

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Temperature Ready | 1 = Temperature measurement is valid | RO | | |

*Table 6.11.148* **Global Thermal Status 2: Address 1E.C821**

### 6.11.149 Global General Status 1: Address 1E.C830

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | 0 | |
| E | High Temperature Failure State | 1 = High-temperature failure threshold has been exceeded | RO | | |
| D | Low Temperature Failure State | 1 = Low-temperature failure threshold has been exceeded | RO | | |
| C | High Temperature Warning State | 1 = High-temperature warning threshold has been exceeded | RO | | |
| B | Low Temperature Warning State | 1 = Low-temperature warning threshold has been exceeded | RO | | |
| A:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.149* **Global General Status 1: Address 1E.C830**

### 6.11.150 Global General Status 2: Address 1E.C831

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Processor-Intensive MDIO Operation In-Progress | 1 = PHY microprocessor is busy with a processor-intensive MDIO operation<br>0 = Processor-intensive MDIO operation completed | RO | | Use bit with certain processor-intensive MDIO commands (Loopbacks, Test Modes, Low power modes, TX-Disable, Restart, Cable Diagnostics, autonegotiation, etc.) that take longer than an MDIO cycle to complete. After receiving an MDIO command that involves the PHY microprocessor, bit is set, and when command completes, is cleared.<br><br>Note, after you launch a processor-intensive MDIO operation, wait for a minimum of 1ms to elapse before checking the bit. The list of operations that set this bit are as follows:<br>1.0.0, PMA Loopback<br>1.0.B, Low power mode<br>1.9.4:0, TX Disable<br>1.84, 10G Test modes<br>1.E400.F, External loopback<br>3.0.B, Low power mode<br>3.0.E, System PCS loopback<br>3.C461.5, PRBS Test (must use XFI0 interface)<br>3.C461.6, PRBS Test (must use XFI0 interface)<br>3.E461.5, PRBS Test (must use XFI0 interface)<br>3.E461.6, PRBS Test (must use XFI0 interface)<br>4.0.B, Low power mode<br>4.0.E, PHY-XS network loopback<br>4.C440, Output clock control, Load SerDes parameters<br>4.F802.E, System loopback<br>4.C444.F:B, Loopback Control<br>4.C444.4:2, Packet generation<br>4.C445.C, SerDes calibration<br>7.0.9, Restart autonegotiation<br>1D.C280, 1G/100M Network loopback<br>1D.C500, 1G System loopback<br>1D.C501, 1G / 100M Test modes<br>1E.C470.4, Cable diagnostics<br>1E.C47A.F:B, Loopback Control<br>1E.C47A.4:2, Packet generation |
| E:0 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.150* **Global General Status 2: Address 1E.C831**

### 6.11.151 Global Pin Status: Address 1E.C840

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | Reserved | Internal reserved - do not modify | | | |
| D | DC_MASTER_N | Value of DC_MASTER_N pin:<br><br>0x1 = Reserved<br>0x0 = PHY Master Daisy Chain Boot from FLASH | RO | | |
| C:A | Reserved | Internal reserved - do not modify | | | |
| 9 | Package Connectivity | Value of the package connection pin | RO | | This is unused. |
| 8 | Reserved | Internal reserved - do not modify | | | |
| 7 | TX Enable | Current Value of TX Enable pin | RO | | This is unused. |
| 6 | Reserved | Internal reserved - do not modify | | | |
| 5:0 | LED Pullup State [5:0] | 1 = LED output pin is pulled high<br>0 = LED output pin is pulled low | RO | | |

*Table 6.11.151* **Global Pin Status: Address 1E.C840**

### 6.11.152 Global Daisy Chain Status 2: Address 1E.C842

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | RX Daisy Chain Calculated CRC [F:0] | RX Daisy Chain Calculated CRC | RO | | This is the calculated Daisy Chain CRC. |

*Table 6.11.152* **Global Daisy Chain Status 2: Address 1E.C842**

### 6.11.153 Global Daisy Chain Hop Count: Address 1E.C84E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved | Internal reserved - do not modify | | | |
| 7:0 | Daisy Chain Hop Count [7:0] | Daisy Chain Hop Count | RO | | This is the configured Daisy Chain hop count. |

*Table 6.11.153* **Global Daisy Chain Hop Count: Address 1E.C84E**

### 6.11.154 Global Fault Message: Address 1E.C850

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Message [F:0] | Error code that describes fault | RO | | Code 0x8001: Firmware *not* compatible with chip architecture. This fault occurs when firmware compiled for a different microprocessor core is loaded.<br>Code 0x8006: Part ID is *not* defined. This can occur if device is *not* properly configured for eFuse.<br>Code 0x8007: PHY thermal shutdown event.<br>Code 0x8008: SFP-DDMI static value FLASH load failure.<br>Code 0x8009: SFP-DDMI SMBus slave address does *not* properly map to memory space.<br>Code 0x9001: Provisioning error.<br>Code 0x9002: Provisioning error in procmon targets.<br>Code 0x9003: Interpreter - Bad training type.<br>Code 0x9004: Interpreter - Uninitialized program section.<br>Code 0x9005: Interpreter - Invalid program section address.<br>Code 0x9006: PLL calibration adjustment - wrong calibration type.<br>Code 0xA002: Unknown state in system-side state machine.<br>Code 0xA003: Unknown state in SerDes state machine.<br>Code 0xA009: Unknown configuration in SIF LED handler.<br>Code 0xA00A: Incorrect SD mode when getting provisioning type.<br>Code 0xA00B: Unknown rate in SIF XFI Init.<br>Code 0xA00C: Unknown target configuration.<br>Code 0xA00D: Provisioning error in SIF init.<br>Code 0xA00E: Unknown SD mode in linkup check.<br>Code 0xA00F: Unknown SD mode in SerDes init.<br>Code 0xA010: SerDes init - PLL locked *not* asserted.<br>Code 0xA011: SerDes calibration - invalid state.<br>Code 0xA012: Unknown state in rate adaptation autoneg state machine.<br>Code 0xA013: Unknown state in SerDes autoneg training state machine.<br>Code 0xA014: Unknown mode in SerDes autoneg training state machine.<br>Code 0xA015: Unknown rate for XGS clock select.<br>Code 0xDEAD: Uncorrectable IRAM parity error.<br>Code 0xDEAE: DRAM parity error.<br>Code 0xDD00: CRC16 IRAM check failure (IRAM load error).<br>Code 0xFACA: eFuse CRC16 check failure (eFuse is corrupted). |

*Table 6.11.154* **Global Fault Message: Address 1E.C850**

### 6.11.155 Global Cable Diagnostic Impedance 1: Address 1E.C880

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved 1 | Reserved | RO | | |
| E:C | Pair A Reflection #1 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the first worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 1: Address 1E.C800" |
| B | Reserved 2 | Reserved | RO | | |
| A:8 | Pair A Reflection #2 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the second worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 1: Address 1E.C800" |
| 7 | Reserved 3 | Reserved | RO | | |
| 6:4 | Pair A Reflection #3 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the third worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 1: Address 1E.C800" |
| 3 | Reserved 4 | Reserved | RO | | |
| 2:0 | Pair A Reflection #4 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the fourth worst reflection on Pair A. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 1: Address 1E.C800" |

*Table 6.11.155* **Global Cable Diagnostic Impedance 1: Address 1E.C880**

### 6.11.156 Global Cable Diagnostic Impedance 2: Address 1E.C881

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved 5 | Reserved | RO | | |
| E:C | Pair B Reflection #1 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the first worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 2: Address 1E.C801" |
| B | Reserved 6 | Reserved | RO | | |
| A:8 | Pair B Reflection #2 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the second worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 2: Address 1E.C801" |
| 7 | Reserved 7 | Reserved | RO | | |
| 6:4 | Pair B Reflection #3 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the third worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 2: Address 1E.C801" |
| 3 | Reserved 8 | Reserved | RO | | |
| 2:0 | Pair B Reflection #4 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the fourth worst reflection on Pair B. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 2: Address 1E.C801" |

*Table 6.11.156* **Global Cable Diagnostic Impedance 2: Address 1E.C881**

### 6.11.157 Global Cable Diagnostic Impedance 3: Address 1E.C882

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved 9 | Reserved | RO | | |
| E:C | Pair C Reflection #1 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the first worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in: "Global Cable Diagnostic Status 3: Address 1E.C802" |
| B | Reserved 10 | Reserved | RO | | |
| A:8 | Pair C Reflection #2 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the second worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" |
| 7 | Reserved 11 | Reserved | RO | | |
| 6:4 | Pair C Reflection #3 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the third worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" |
| 3 | Reserved 12 | Reserved | RO | | |
| 2:0 | Pair C Reflection #4 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the fourth worst reflection on Pair C. The corresponding length of this reflection from the PHY is given in "Global Cable Diagnostic Status 3: Address 1E.C802" |

*Table 6.11.157* **Global Cable Diagnostic Impedance 3: Address 1E.C882**

### 6.11.158 Global Cable Diagnostic Impedance 4: Address 1E.C883

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved 13 | Reserved | RO | | |
| E:C | Pair D Reflection #1 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the first worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in:<br>"Global Cable Diagnostic Status 4: Address 1E.C803" |
| B | Reserved 14 | Reserved | RO | | |
| A:8 | Pair D Reflection #2 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx = No information available | RO | | The impedance of the second worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in:<br>"Global Cable Diagnostic Status 4: Address 1E.C803" |
| 7 | Reserved 15 | Reserved | RO | | |
| 6:4 | Pair D Reflection #3 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the third worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in:<br>"Global Cable Diagnostic Status 4: Address 1E.C803" |
| 3 | Reserved 16 | Reserved | RO | | |
| 2:0 | Pair D Reflection #4 [2:0] | 111 = Open Circuit (> 300Ω)<br>110 = High Mismatch (> 115Ω)<br>101 = Low Mismatch (< 85Ω)<br>100 = Short Circuit (< 30Ω)<br>0xx= No information available | RO | | The impedance of the fourth worst reflection on Pair D. The corresponding length of this reflection from the PHY is given in:<br>"Global Cable Diagnostic Status 4: Address 1E.C803" |

*Table 6.11.158* **Global Cable Diagnostic Impedance 4: Address 1E.C883**

### 6.11.159 Global Status: Address 1E.C884

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved Status 0 [7:0] | Reserved | RO | | |
| 7:0 | Cable Length [7:0] | Estimated length of cable in meters | RO | | The length of the cable shown here is estimated from the cable diagnostic engine and should be accurate to +/-1m. |

*Table 6.11.159* **Global Status: Address 1E.C884**

### 6.11.160 Global Reserved Status 1: Address 1E.C885

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:A | Nearly Seconds MSW[5:0] | Bits 16 to 21 of the 22-bit “Nearly Seconds” uptime counter | RO | | The “Nearly Seconds” counter is incremented every 1024 milliseconds. |
| 9:8 | NVR Status [1:0] | Status of NVR:<br>0: NVR *not* enabled<br>1: Last NVR operation succeeded<br>2: Last NVR operation failed<br>3: Reserved | ROS PD | 0x0 | Register space is mirrored in NVR (SPI ROM), and this register indicates the status of the last NVR operation. |

*Table 6.11.160* **Global Reserved Status 1: Address 1E.C885**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7:4 | Firmware Build ID [3:0] | Firmware Build ID | ROS PD | 0x0 | Customers may receive multiple ROM images that differ only in their provisioning. This field helps to differentiate the images and is used in conjunction with the firmware major and minor revision version numbers to uniquely identify the ROM images. |
| 3:0 | Provisioning ID [3:0] | Provisioning ID | ROS PD | 0x0 | Customers may receive multiple ROM images that differ only in their provisioning. This field helps to differentiate the images and is used in conjunction with the firmware major and minor revision version numbers to uniquely identify the ROM images. |

*Table 6.11.160* **Global Reserved Status 1: Address 1E.C885** (continued)

### 6.11.161 Global Reserved Status 2: Address 1E.C886

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Nearly Seconds LSW [F:0] | Bits 0 to 15 of the 22 bit “Nearly Seconds” uptime counter | RO | | The “Nearly Seconds” counter is incremented every 1024 milliseconds. |

*Table 6.11.161* **Global Reserved Status 2: Address 1E.C886**

### 6.11.162 Global Reserved Status 3: Address 1E.C887

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | DTE Status | 1 = Needs power<br>0 = Does not need power | ROS | 0 | |
| E | Power-Up Stall Status | 1 = Firmware is stalled at power-up<br>0 = Firmware is not stalled | ROS | 0 | |
| D:0 | Reserved Status 3 [D:0] | Reserved for future use | RO | | |

*Table 6.11.162* **Global Reserved Status 3: Address 1E.C887**

### 6.11.163 Global Reserved Status 4: Address 1E.C888

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:B | Loopback Status [4:0] | 0x00 = No loopback<br>0x01 = System Interface - System Loopback<br>0x02 = System Interface - System Loopback with Passthrough<br>0x03 = System Interface - Network Loopback<br>0x04 = System Interface - Network Loopback with Passthrough<br>0x05 = System Interface - Network Loopback with Passthrough and Merge<br>0x06 = System Interface - Peer-to-peer loopback<br>0x07 - 0x08 = Reserved<br>0x09 = Network Interface - System Loopback<br>0x0A = Network Interface - System Loopback with Passthrough<br>0x0B = Network Interface - Network Loopback<br>0x0C = Network Interface - Network Loopback with Passthrough<br>0x0D = Network Interface - Peer-to-peer loopback<br>0x0E - 0x0F = Reserved<br>0x10 = Cross-connect System Loopback<br>0x11 = Cross-connect Network Loopback<br>0x12 - 0x13 = Reserved<br>0x14 = Network Interface - System Loopback via Loopback Plug<br>0x15 - 0x1F = Reserved | RO | | These bits, in conjunction with the chip configuration and the rate (Bits 1:0), report the selected loopback. |
| A:6 | Reserved Status 4 [4:0] | Reserved for future use | RO | | |

*Table 6.11.163* **Global Reserved Status 4: Address 1E.C888**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5 | MDI Packet Generation Status | 1 = CRPAT packet generation out MDI interface<br>0 = No CRPAT packet generation out MDI interface | RO | | Reports if the CRPAT packet generator in the PHY outputs on the MDI interface at the selected rate. |
| 4 | Look-Aside Port Packet Generation Status | 1 = CRPAT packet generation out 10G look-aside interface (KR0)<br>0 = No CRPAT packet generation out 10G look-aside interface (KR0) | RO | | Reports if the CRPAT packet generator in the PHY outputs on the KR0 interface at the selected rate. |
| 3 | System I/F Packet Generation Status | 1 = CRPAT packet generation out 10G system interface<br>0 = No CRPAT packet generation out 10G system interface | RO | | Reports if the CRPAT packet generator in the PHY outputs on the selected system interface at the selected rate. |
| 2:0 | Rate [2:0] | 0x7 - 0x6 = reserved<br>0x5 = 5G<br>0x4 = 2.5G<br>0x3 = 10G<br>0x2 = 1G<br>0x1 = 100M<br>0x0 = invalid | RO | | These bits report the selected rate for the loopback and packet generation. |

*Table 6.11.163* **Global Reserved Status 4: Address 1E.C888** (continued)

### 6.11.164 Global Reserved Status 5: Address 1E.C889

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Status 5 [F:0] | Reserved for future use | RO | | |

*Table 6.11.164* **Global Reserved Status 5: Address 1E.C889**

### 6.11.165 Global Reserved Status 6: Address 1E.C88A

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Status 6 [F:0] | Reserved for future use | RO | | |

*Table 6.11.165* **Global Reserved Status 6: Address 1E.C88A**

### 6.11.166 Global Reserved Status 7: Address 1E.C88B

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Status 7 [F:0] | Reserved for future use | RO | | |

*Table 6.11.166* **Global Reserved Status 7: Address 1E.C88B**

### 6.11.167 Global Reserved Status 8: Address 1E.C88C

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Reserved Status 8 [F:0] | Reserved for future use | RO | | |

*Table 6.11.167* **Global Reserved Status 8: Address 1E.C88C**

### 6.11.168 Global Reserved Status 9: Address 1E.C88D

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:8 | Reserved Status 9 [7:0] | Reserved for future use | ROS PD | 0x00 | |
| 7:4 | Resolved Constellation [3:0] | 0 = Invalid<br>1 = PAM16<br>2 = DSQ 128<br>3 = DSQ128RS<br>4 = SQ64<br>5 = 1000BaseT<br>6 = 100BaseT | ROS PD | 0x0 | |
| 3:0 | Resolved Active Lane Capability [3:0] | Resolved Active Lane Mask<br>0x1 = 1 Pair mode<br>0x3 = 2 Pair Mode<br>0xF = 4 Pair Mode | ROS PD | 0x0 | |

*Table 6.11.168* **Global Reserved Status 9: Address 1E.C88D**

### 6.11.169 Global Reserved Status 10: Address 1E.C88E

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Resolved Baud Rate [F:0] | Baud rate in Mega Symbols/sec | ROS PD | 0x0000 | |

*Table 6.11.169* **Global Reserved Status 10: Address 1E.C88E**

### 6.11.170 Global Reserved Status 11: Address 1E.C88F

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:0 | Customer Provisioning ID [F:0] | | ROS PD | 0x0000 | |

*Table 6.11.170* **Global Reserved Status 11: Address 1E.C88F**

### 6.11.171 Global Alarms 1: Address 1E.CC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | 0 | |
| E | High Temperature Failure | 1 = High temperature failure threshold has been exceeded | LH | | These bits mirror the matching bit in 1.A070 and 1.A074, are driven by Bits E:B in “Global General Status 1: Address 1E.C830” on page 554. |
| D | Low Temperature Failure | 1 = Low temperature failure threshold has been exceeded | LH | | |
| C | High Temperature Warning | 1 = High temperature warning threshold has been exceeded | LH | | |
| B | Low Temperature Warning | 1 = Low temperature warning threshold has been exceeded | LH | | |
| A:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Reset completed | 1 = Chip wide reset completed | LH | | This bit is set by the microprocessor when it has completed it’s initialization sequence, and bit is mirrored in 1.CC02.0 |
| 5 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.171* **Global Alarms 1: Address 1E.CC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4 | Device Fault | 1 = Fault | LH | | When set, a fault has been detected by the uP and the associated 16 bit error code is visible in Global Fault Message: Address 1E.C850 |
| 3 | Reserved Alarm A | Reserved for future use | LH | | |
| 2 | Reserved Alarm B | Reserved for future use | LH | | |
| 1 | Reserved Alarm C | Reserved for future use | LH | | |
| 0 | Reserved Alarm D | Reserved for future use | LH | | |

*Table 6.11.171* **Global Alarms 1: Address 1E.CC00** (continued)

### 6.11.172 Global Alarms 2: Address 1E.CC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | Smart Power-Down Entered | 1 = Smart Power-Down State Entered | LH | | When bit is set, indicates that the Smart Power-Down state was entered. |
| D | Alarm | 1 = Alarm | RO | | |
| C | IP Phone Detect | 1 = IP Phone Detect | LH | | Assertion of this bit means that the presence of an IP phone has been detected. |
| B | DTE Status Change | 1 = DTE status change | LH | | Change in 1E.C887[F]. |
| A | Fast Link Drop | 1 = PHY has entered link recovery state | LH | | This alarm is asserted before entering the PHY link recovery state. This alarm can be used as an early sign for a link drop in case of an unsuccessful link recovery. |
| 9 | SFP DDMI Memory Load Failed | 1 = PHY failed to load static values from FLASH for the SFP-DDMI memory maps | LH | | When PHY firmware is used to implement the SFP Digital Diagnostic Monitoring Interface via the SMB0 SMBus controller, static values for memory maps are loaded from FLASH during initialization. If this load fails, this alarm is set. |
| 8 | SMB0 State Machine Timeout | 1 = Firmware SMB0 management state machine timed out | LH | | This alarm indicates that the firmware state machine that manages the SMB0 controller as a slave SMBus device was forced back to its idle state. This can happen when the controller receives an unexpected or invalid input sequence from the bus master. |

*Table 6.11.172* **Global Alarms 2: Address 1E.CC01**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 7 | MDIO Command Handling Overflow | 1 = PHY was issued more MDIO requests than it could service in its request buffer | LH | | Assertion of this bit means that more MDIO commands were issued than firmware could handle. |
| 6:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Diagnostic Alarm | 1 = Alarm triggered by a write to 1E.C470.7 | LH | | Indicates that a diagnostic alarm was used to test system alarm circuitry. |

*Table 6.11.172* **Global Alarms 2: Address 1E.CC01** (continued)

### 6.11.173 Global Alarms 3: Address 1E.CC02

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | NVR Operation Complete | 1 = NVR operation is complete | LH | | NVR interface is ready interrupt for registers:<br><br>Global NVR Interface 1: Address 1E.100 - Global NVR Interface 5: Address 1E.104 |
| E | Mailbox Operation: Complete | 1 = Mailbox operation is complete | LH | | Mailbox interface is ready interrupt for registers:<br><br>Global Mailbox Interface 1: Address 1E.200 - Global Mailbox Interface 5: Address 1E.204 |
| D:C | Reserved | Internal reserved - do not modify | | | |
| B:A | uP DRAM Parity Error [1:0] | 1 = Parity error detected in the uP DRAM | LH | | Bit 0 indicates a parity error was detected in the uP DRAM, but was corrected.<br><br>Bit 1 indicates a multiple parity errors were detected in the uP DRAM and could *not* be corrected.<br><br>**Note:** The uP DRAM is protected with ECC. |
| 9:8 | uP IRAM Parity Error [1:0] | 1 = Parity error detected in the uP IRAM | LH | | Bit 0 indicates a parity error was detected in the uP IRAM but was corrected.<br><br>Bit 1 indicates a multiple parity errors were detected in the uP IRAM and could *not* be corrected.<br><br>**Note:** The uP IRAM is protected with ECC. |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | TX Enable State Change | 1 = TX_EN pin has changed state | LRF | | This is unused. |

*Table 6.11.173* **Global Alarms 3: Address 1E.CC02**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 4:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | MDIO MMD Error | 1 = Invalid MMD address detected | LH | | |
| 1 | MDIO Timeout Error | 1 = MDIO timeout detected | LH | | |
| 0 | Watchdog Timer Alarm | 1 = Watchdog timer alarm | LH | | |

*Table 6.11.173* **Global Alarms 3: Address 1E.CC02** (continued)

### 6.11.174 Global Interrupt Mask 1: Address 1E.D400

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | High Temperature Failure Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| D | Low Temperature Failure Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | High Temperature Warning Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B | Low Temperature Warning Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| A:7 | Reserved | Internal reserved - do not modify | | | |
| 6 | Reset completed Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 5 | Reserved | Internal reserved - do not modify | | | |
| 4 | Device Fault Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 3 | Reserved Alarm A Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 2 | Reserved Alarm B Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.174* **Global Interrupt Mask 1: Address 1E.D400**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 1 | Reserved Alarm C Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 0 | Reserved Alarm D Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.174* **Global Interrupt Mask 1: Address 1E.D400** (continued)

### 6.11.175 Global Interrupt Mask 2: Address 1E.D401

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Internal reserved - do not modify | | | |
| E | Smart Power-Down Entered Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| D | Alarm Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | IP Phone Detect Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B | DTE Status Change Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| A | Fast Link Drop Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 9 | SFP DDMI Memory Load Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.175* **Global Interrupt Mask 2: Address 1E.D401**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 8 | SMB0 State Machine Timeout Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 7 | MDIO Command Handling Overflow Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 6:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | Diagnostic Alarm Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.175* **Global Interrupt Mask 2: Address 1E.D401** (continued)

### 6.11.176 Global Interrupt Mask 3: Address 1E.D402

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | NVR Operation Complete Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | NVR interface is ready interrupt for registers:<br><br>Global NVR Interface 1: Address 1E.100 - Global NVR Interface 5: Address 1E.104 |
| E | Mailbox Operation Complete Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | Mailbox interface is ready interrupt for registers:<br><br>Global Mailbox Interface 1: Address 1E.200 - Global Mailbox Interface 5: Address 1E.204 |
| D:C | Reserved | Internal reserved - do not modify | | | |
| B:A | uP DRAM Parity Error Mask [1:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0x0 | |
| 9:8 | uP IRAM Parity Error Mask [1:0] | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0x0 | |
| 7:6 | Reserved | Internal reserved - do not modify | | | |
| 5 | TX Enable State Change Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 4:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | MDIO MMD Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 1 | MDIO Timeout Error Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 0 | Watchdog Timer Alarm Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.176* **Global Interrupt Mask 3: Address 1E.D402**

### 6.11.177 Global Chip-Wide Standard Interrupt Flags: Address 1E.FC00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PMA Standard Alarm 1 Interrupt | 1 = Interrupt in PMA standard alarms 1 | RO | | An interrupt was generated from bit 1.1.2. An interrupt was generated from status register (see “PMA Standard Status 1: Address 1.1” on page 134) and the corresponding mask register (see “PMA Transmit Standard Interrupt Mask 1: Address 1.D000” on page 163). |
| E | PMA Standard Alarm 2 Interrupt | 1 = Interrupt in PMA standard alarms 2 | RO | | An interrupt was generated from either bit 1.8.B or 1.8.A. An interrupt was generated from status register (see “PMA Standard Status 2: Address 1.8” on page 140) and the corresponding mask register (see “PMA Transmit Standard Interrupt Mask 2: Address 1.D001” on page 164). |
| D | PCS Standard Alarm 1 Interrupt | 1 = Interrupt in PCS standard alarms 1 | RO | | An interrupt was generated from status register (see “PCS Standard Status 1: Address 3.1” on page 173) and the corresponding mask register (see “PCS Standard Interrupt Mask 1: Address 3.D000” on page 244). |
| C | PCS Standard Alarm 2 Interrupt | 1 = Interrupt in PCS standard alarms 2 | RO | | An interrupt was generated from status register (see “PCS Standard Status 2: Address 3.8” on page 178) and the corresponding mask register (see “PCS Standard Interrupt Mask 2: Address 3.D001” on page 244). |
| B | PCS Standard Alarm 3 Interrupt | 1 = Interrupt in PCS standard alarms 3 | RO | | An interrupt was generated from status register (see “PCS 10G Status 2: Address 3.21” on page 184) and the corresponding mask register (see “PCS Standard Interrupt Mask 3: Address 3.D002” on page 245). |

*Table 6.11.177* **Global Chip-Wide Standard Interrupt Flags: Address 1E.FC00**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| A | PHY XS Standard Alarms 1 Interrupt | 1 = Interrupt in PHY XS standard alarms 1 | RO | | An interrupt was generated from the status register (see “PHY XS Standard Status 1: Address 4.1” on page 302) and the corresponding mask register (see “PHY XS Transmit (XAUI RX) Standard Interrupt Mask 1: Address 4.D000” on page 330). |
| 9 | PHY XS Standard Alarms 2 Interrupt | 1 = Interrupt in PHY XS standard alarms 2 | RO | | An interrupt was generated from the status register (see “PHY XS Standard Status 2: Address 4.8” on page 307) and the corresponding mask register (see “PHY XS Transmit (XAUI RX) Standard Interrupt Mask 2: Address 4.D001” on page 331). |
| 8 | Autonegotiation Standard Alarms 1 Interrupt | 1 = Interrupt in Autonegotiation standard alarms 1 | RO | | An interrupt was generated from status register (see “Autonegotiation Standard Status 1: Address 7.1” on page 354) and the corresponding mask register (see “Autonegotiation Standard Interrupt Mask 1: Address 7.D000” on page 406). |
| 7 | Autonegotiation Standard Alarms 2 Interrupt | 1 = Interrupt in Autonegotiation standard alarms 2 | RO | | An interrupt was generated from status register (see “Autonegotiation 10GBASE-T Status Register: Address 7.21” on page 367) and the corresponding mask register (see “Autonegotiation Standard Interrupt Mask 2: Address 7.D001” on page 406). |
| 6 | GbE Standard Alarms Interrupt | 1 = Interrupt in GbE standard alarms | RO | | An interrupt was generated from the TGE core. |

*Table 6.11.177* **Global Chip-Wide Standard Interrupt Flags: Address 1E.FC00** (continued)

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 5:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | All Vendor Alarms Interrupt | 1 = Interrupt in all vendor alarms | RO | | An interrupt was generated from status register (see “Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01” on page 582) and the corresponding mask register (see “Global Interrupt Chip-Wide Vendor Mask: Address 1E.FF01” on page 585). |

*Table 6.11.177* **Global Chip-Wide Standard Interrupt Flags: Address 1E.FC00** (continued)

### 6.11.178 Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PMA Vendor Alarm Interrupt | 1 = Interrupt in PMA vendor specific alarm | RO | | A PMA alarm was generated (see “PMA Vendor Global Interrupt Flags 1: Address 1.FC00” on page 168). |
| E | PCS Vendor Alarm Interrupt | 1 = Interrupt in PCS vendor specific alarm | RO | | A PCS alarm was generated (see “PCS Vendor Global Interrupt Flags 1: Address 3.FC00” on page 299). |
| D | PHY XS Vendor Alarm Interrupt | 1 = Interrupt in PHY XS vendor specific alarm | RO | | A PHY XS alarm was generated (see “PHY XS Vendor Global Interrupt Flags 1: Address 4.FC00” on page 352). |
| C | Autonegotiation Vendor Alarm Interrupt | 1 = Interrupt in Autonegotiation vendor specific alarm | RO | | An Autonegotiation alarm was generated (see “Autonegotiation Vendor Global Interrupt Flags 1: Address 7.FC00” on page 418). |
| B | GbE Vendor Alarm Interrupt | 1 = Interrupt in GbE vendor specific alarm | RO | | A GbE alarm was generated (see “GbE PHY Vendor Global Interrupt Flags 1: Address 1D.FC00” on page 474). |
| A:3 | Reserved | Internal reserved - do not modify | | | |

*Table 6.11.178* **Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01**

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| 2 | Global Alarms 1 Interrupt | 1 = Interrupt in Global alarms 1 | RO | | An interrupt was generated from status register (see “Global Alarms 1: Address 1E.CC00” on page 570) and the corresponding mask register (see “Global Interrupt Mask 1: Address 1E.D400” on page 576). |
| 1 | Global Alarms 2 Interrupt | 1 = Interrupt in Global alarms 2 | RO | | An interrupt was generated from status register (see “Global Alarms 2: Address 1E.CC01” on page 572) and the corresponding mask register (see “Global Interrupt Mask 2: Address 1E.D401” on page 577). |
| 0 | Global Alarms 3 Interrupt | 1 = Interrupt in Global alarms 3 | RO | | An interrupt was generated from status register (see “Global Alarms 3: Address 1E.CC02” on page 574) and the corresponding mask register (see “Global Interrupt Mask 3: Address 1E.D402” on page 579). |

*Table 6.11.178* **Global Chip-Wide Vendor Interrupt Flags: Address 1E.FC01** (continued)

### 6.11.179 Global Interrupt Chip-Wide Standard Mask: Address 1E.FF00

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PMA Standard Alarm 1 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| E | PMA Standard Alarm 2 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| D | PCS Standard Alarm 1 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | PCS Standard Alarm 2 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B | PCS Standard Alarm 3 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| A | PHY XS Standard Alarms 1 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 9 | PHY XS Standard Alarms 2 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 8 | Autonegotiation Standard Alarms 1 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 7 | Autonegotiation Standard Alarms 2 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 6 | GbE Standard Alarms Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 5:1 | Reserved | Internal reserved - do not modify | | | |
| 0 | All Vendor Alarms Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.179* **Global Interrupt Chip-Wide Standard Mask: Address 1E.FF00**

### 6.11.180 Global Interrupt Chip-Wide Vendor Mask: Address 1E.FF01

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | PMA Vendor Alarm Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| E | PCS Vendor Alarm Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| D | PHY XS Vendor Alarm Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| C | Autonegotiation Vendor Alarm Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| B | GbE Vendor Alarm Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| A:3 | Reserved | Internal reserved - do not modify | | | |
| 2 | Global Alarms 1 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 1 | Global Alarms 2 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |
| 0 | Global Alarms 3 Interrupt Mask | 1 = Enables interrupt generation<br>0 = Disables interrupt generation | R/W PD | 0 | |

*Table 6.11.180* **Global Interrupt Chip-Wide Vendor Mask: Address 1E.FF01**

# 6.12 SEC Ingress and Egress Registers

### 6.12.1 SEC Ingress Control Register 1: Address 1E.7000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Value always 0, writes are ignored | | | |
| D | Reserved | Value always 0, writes are ignored | | | |
| C | Reserved | Value always 0, writes are ignored | | | |
| B | Reserved | Value always 0, writes are ignored | | | |
| A:7 | Reserved | Value always 0, writes are ignored | | | |
| 6 | Reserved | Value always 0, writes are ignored | | | |
| 5 | Reserved | Value always 0, writes are ignored | | | |
| 4:0 | Reserved | Value always 0, writes are ignored | | | |

*Table 6.12.1* **SEC Ingress Control Register 1: Address 1E.7000**

### 6.12.2 SEC Ingress Control Register 2: Address 1E.7001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Value always 0, writes are ignored | | | |
| E | Reserved | Value always 0, writes are ignored | | | |
| D | Reserved | Value always 0, writes are ignored | | | |
| C | Reserved | Value always 0, writes are ignored | | | |
| B | Reserved | Value always 0, writes are ignored | | | |
| A:8 | SEC Ingress EEE Mode [2:0] | Indicates EEE Mode | R/W | 0x0 | 0x1: MAC-controlled EEE<br>0x2: PHY-controlled EEE<br>0x4: MDIO-generated EEE<br><br>In internally generated EEE mode, if the ingress FC FIFO is empty for a configurable time, the system-side MAC TX will insert LPI. |
| 7 | Reserved | Value always 0, writes are ignored | | | |
| 6 | Reserved | Value always 0, writes are ignored | | | |
| 5 | Reserved | Value always 0, writes are ignored | | | |
| 4 | Reserved | Value always 0, writes are ignored | | | |
| 3 | Reserved | Value always 0, writes are ignored | | | |
| 2 | Reserved | Value always 0, writes are ignored | | | |
| 1 | Reserved | Value always 0, writes are ignored | | | |
| 0 | Reserved | Value always 0, writes are ignored | | | |

*Table 6.12.2* **SEC Ingress Control Register 2: Address 1E.7001**

### 6.12.3 SEC Egress Control Register 1: Address 1E.4000

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F:E | Reserved | Value always 0, writes are ignored | | | |
| D | SEC Egress Shallow Loopback Enable | 1 = Enables shallow loopback | R/W | 0 | When this bit is set to 1, the line-side MAC loopback is enabled (for example, the line-side MAC RX data is sent to the line-side MAC TX data). |
| C | SEC Egress Bypass Enable | 1 = Bypasses all SEC blocks | R/W | 0 | When this bit is set to 1, all the egress SEC blocks (including FC FIFO, PKT, PTP and MSS) are bypassed (for example, the system-side MAC RX data is sent to the line-side MAC TX data). |
| B | SEC Egress Bypass MSS Enable | 1 = Bypasses MSS block | R/W | 0 | When this bit is set to 1, the egress MSS block is bypassed (for example, the egress PTP data is sent to the line-side MAC without encryption). |
| A:7 | Reserved | Value always 0, writes are ignored | | | |
| 6 | SEC Egress Tail Drop Enable | 1 = Enables tail drop | R/W | 0 | When this bit is set to 1, the last packet is dropped when the egress FC FIFO becomes full.<br><br>When this bit is set to 0, the last packet can be truncated when the egress FIFO becomes full. |
| 5 | SEC Egress Store Forward Enable | 1 = Enables store and forward | R/W | 0 | When this bit is set to 1, the egress FC FIFO is read-only after a full packet is written into the FIFO. |
| 4:0 | Reserved | Value always 0, writes are ignored | | | |

*Table 6.12.3* **SEC Egress Control Register 1: Address 1E.4000**

### 6.12.4 SEC Egress Control Register 2: Address 1E.4001

| Bit | Name | Description | Type | Default | Note |
|---|---|---|---|---|---|
| F | Reserved | Value always 0, writes are ignored | | | |
| E | Reserved | Value always 0, writes are ignored | | | |
| D | Reserved | Value always 0, writes are ignored | | | |
| C | Reserved | Value always 0, writes are ignored | | | |
| B | Reserved | Value always 0, writes are ignored | | | |
| A:8 | SEC Egress EEE Mode [2:0] | Indicates the EEE Mode | R/W | 0x0 | 0x1: MAC-controlled EEE.<br>0x2: PHY-controlled EEE.<br>0x4: MDIO-generated EEE.<br><br>In an internally generated EEE mode, if the egress FC FIFO is empty for a configurable time, the line-side MAC TX inserts an LPI. |
| 7 | Reserved | Value always 0, writes are ignored | | | |
| 6 | Reserved | Value always 0, writes are ignored | | | |
| 5 | Reserved | Value always 0, writes are ignored | | | |
| 4 | Reserved | Value always 0, writes are ignored | | | |
| 3 | Reserved | Value always 0, writes are ignored | | | |
| 2 | Reserved | Value always 0, writes are ignored | | | |
| 1 | Reserved | Value always 0, writes are ignored | | | |
| 0 | Reserved | Value always 0, writes are ignored | | | |

*Table 6.12.4* **SEC Egress Control Register 2: Address 1E.4001**

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